VT-1100A/1105A/1310A/1305A

HITACHI
SERVICE MANUAL

TK | No. 2508E

VT-1100A/1105A
1310A/1305A

Technical Information

VHS

THIS VIDEO DECK IS A VHS TYPE VIDEO RECORDER.
FOR PROPER OPERATION, ONLY THE VHS TYPE CASSETTE MUST BE USED.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

VIDEO CASSETTE RECORDER

June 1986 **TOKAI WORKS**

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Y CHASSIS SYSTEM CONSISTENCY

The following table shows the differences from X chassis system consistency on Y chassis VTR.

#	ISSUE	(X) CHASSIS	(Y) CHASSIS	
1	Tape speed selector	The selector is lock type switch	The SW is momentary type, and the default value is EP when AC is plugged in.	
2	At the index mark when VTR is rewind and IRT is set.	There are two type 1) Continue to rewind. 2) Start IRT	Continue to rewind.	
3	Memory on/off and counter clear operation	1) It's always allowed whether the display shows tape remain or counter. 2) It's allowed only when the counter is displayed.	OSD Counter Model It's always allowed. FL Counter Model It's allowed only when the counter is displayed.	
4	Memory stop	1) The VTR stops only when the display mode is counter and memory is on. 2) The VTR always stop when memory is on.	The VTR always stop when memory is on.	
5	Timer program menu of 4-program/ 2-week Timer	Three normal/daily programs and one weekly program.	All the 4 programs are free to program as normal, weekly or daily.	**
6	50/60Hz AC clock base decision	Only one time when AC cord is plugged in.	All the time in every clock pulses.	**
7	Memory stop mode	Rew, A.dub, V.dub	Few, A.dub, V.dub and F.FWD	**
8	Index mark recording for continuous Timer program	The VTR unloads tape at the boundary of Timer Program, then loads tape and writes index mark.	Without unloading, the VTR can write index mark at the boundary of Timer program.	**
9	Start of Timer program & IRT	The VTR begins recording at just start time.	The VTR begins recording at 5 sec before the start time.	**
10	Clock setting operation	Push both CLOCK & ENTER buttons.	Push CLOCK button first, then one finger operation is possible.	**
11	Local slow operation	No way without SLOW button.	Push PLAY button under still picture.	**

** New item.

DIFFERENCE BETWEEN VT-63A and VT-1100A/1105A (CIRCUIT)

ITEM \ MODEL		VT-63A	VT-1100A/1105A
CHASSIS		X	Y
LUMA	H Q	NO	YES
	DOC (ELEMENT)	FM (GLASS)	VIDEO (CCD)
CHROMA			(IC IS CHANGED)
CYLINDER	SHAPE		MOUNT TYPE OF PRE-AMP
	VIDEO HEAD	2 HEADS	2 HEADS
	MOTOR	SINGLE PHASE	3-PHASE
SERVO	SLOW	NONE	NONE
	STILL	FRAME	FRAME
	F. ADV.	NONE	NONE
	NOISE LOCK SEARCH	NONE	YES
SYSTEM	MODE DISPLAY	YES (LED)	YES (LED)
	TAPE SPEED DISPLAY	YES (LED)	YES (FL)
	TAPE SPEED SWITCH	SLIDE	TACT
	CLOCK BUTTON	HOLD TYPE	TACT TYPE
	POWER LED	YES	YES
TUNER	SHAPE	UNIT TYPE	MOUNTED ON P.C.B
CABINET	MATERIAL	PLASTIC	METAL

1. POWER SUPPLY

Fig. 1-1 and 1-2 show the generation circuits of power sources necessary for the various circuits in the VT-1100A. The power generation circuits are located on four circuit board assemblies - REG/CYL MOTOR DRIVE, U/V TUNING, TIMER INPUT KEY and MAIN.
These power sources can be roughly divided into two.

- 9 power sources generated when power is supplied to the VTR: AC4V, A30V, A-30V, A5.6V, BU5V, A5V, A18V, M12V, A12V.
- 3 power sources generated when the power switch is turned ON: 5V, 10V, 12V.

Table 1-1 shows the specifications and applications of these 12 power sources.

POWER ON/OFF

The power sources, 5V, 10V and 12V, which are generated when the power switch is turned ON are switched ON/OFF by system control μP (IC901: S-μP). To perform this control, the S-μP receives the operation data of power switch (S111: Push-type Switch) as shown in Fig. 1-2, input to timer μP (IC751: T-μP or TI-μP), via the communications lines. S-μP turns the output of the power holding memory in the IC to ON and OFF alternately every time S-μP receives data. The memory output is derived from pin 6 and goes "Hi" when the power switch is turned ON. The output (Hi) at pin 6 turns on the 12V B+ Switches (Q851, Q852). This causes the A12V source to be output via Q852. This output becomes a 12V power source. This 12V source is dropped by 1.8V to 10.2V via the voltage drop diodes (D502 - D505), thus the 10V source is produced. The 12V power source is also applied to pin 2 of 5V regulator (IC851). This activates the 5V regulator and the 5V source is output from pin 1.

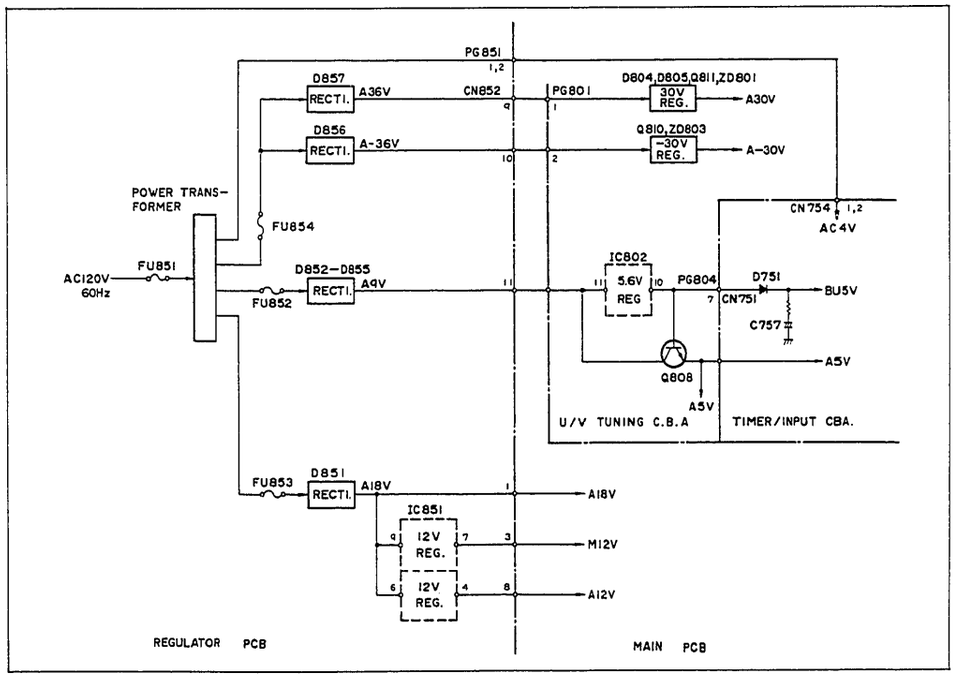


Fig. 1-1 Simplified Power Supply (Always) Circuit Diagram

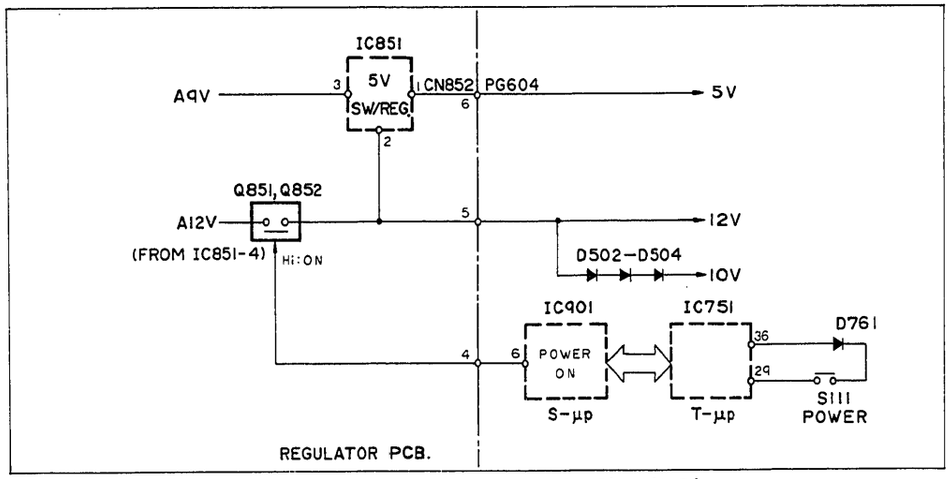


Fig. 1-2 Simplified Switched Power Supply Circuit Diagram

	Power supply	Voltage	Generator (location)	Active Mode	Application
1	AC4V	AC4.1V (Unregulated)	Power transformer (REG)	Always	Heater in digital multi-display
2	A30V	30V (Regulated)	Cathode of ZD801 (U/V TUNING)	Always	Tuning voltage generator circuit
3	A-30V	-30V (Regulated)	Emitter of Q810 (U/V TUNING)	Always	EAROM and timer μP for digital multidisplay
4	A5.6V	5.6V (Regulated)	Pin 10 of IC802 (U/V TUNING)	Always	IR receiver
5	BU5V	5V (Regulated)	C758/759 (TIMER)	Always	Timer μP (This power supply is backed up by C758/759 for approx. 1 sec.)
6	A5V	5V (Regulated)	Emitter of Q808 (U/V TUNING)	Always	9 LEDs, EAROM, tuning μP and system control μP
7	5V	5V (Regulated)	Pin 1 of IC851 (REG)	Power ON	Servo & Luminance/Chroma process IC, cylinder motor drive
8	A18V	18V (Unregulated)	Cathode of D3 (REG)	Always	Capstan motor drive
9	M12V	12V (Regulated)	Pin 7 of IC851 (REG)	Always	Loading and cylinder motor drivers
10	A12V	12V (Regulated)	PIN 4 of IC851 (REG)	Always	Loading motor driver & end lamp
11	10V	10.2V (Regulated)	Cathode of D504	Power ON	CCD 1H delay line on luminance/chroma board
12	12V	12V (Regulated)	Collector of Q851 (REG)	Power ON	Tuner, video input selector, RF converter, audio process IC

Table 1-1 Power Supply

2. SYSTEM CONTROL

2-1 General

The system control circuit inputs the commands given by the operator and sets the mechanism and circuits to the commanded mode. The circuit also inputs the detection outputs from the tape/mechanism protection sensors and protects the VTR and tape against abnormal operations. Fig. 2-1 is a simplified system control diagram. System control is performed by 3 microprocessors (system control μP: S-μP, timer μP: T-μP, tuning μP: TU-μP). S-μP communicates commands given by the operator and information of VTR operation modes, etc. with T-μP, and T-μP communicates with TU-μP. The μP controls the following according to this information.

S-μP: 1. Sets the mechanism, servo, audio/video processing and power supply circuits to the commanded mode according to two types of switch operation data (1: Function switches input by T-μP, 2: Remote function switches input by TU-μP) and timer outputs.

2. Sets the VTR to the stop mode according to the detection outputs of trouble sensors in the mechanism and servo circuit and protects the VTR and tape against abnormal operation.

3. Transmits the VTR operation mode data to T-μP to drive the indicators (STOP and PAUSE etc.) and digital multidisplay and informs the operator of the VTR operation state.

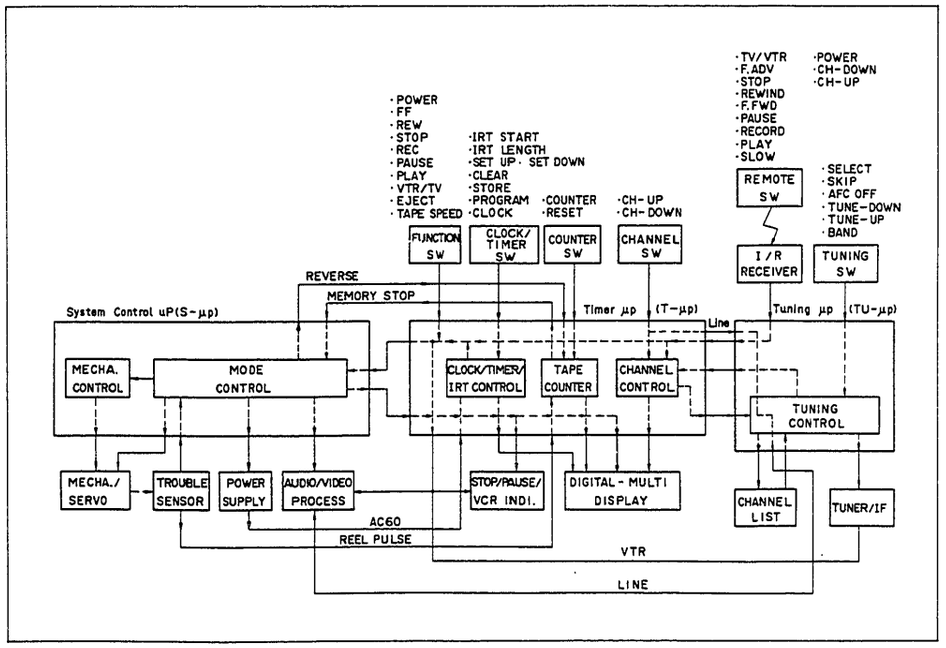


Fig. 2-1 System Control Block Diagram

4. Transmits the tape running direction data to the counter in T-μP to determine the counter mode.
5. Receives the memory stop data from T-μP and sets the VTR to the stop mode.

The data required in 1 - 3 above is transmitted and received via communications lines between the μPs.

T-μP: 1. Receives the function switch operation data and transmits the data to S-μP via the communications lines; S-μP determines the VTR operation mode according to the data.
2. Receives the clock/timer switch operation data and supplies it to the internal power frequency counter for the clock/timer/IRT. Using the data, the counter determines display switching, the present time, timer ON/OFF times and IRT ON/OFF times.
3. Receives the counter switch operation data and supplies it to the internal tape counter to switch the display between clock and counter and to reset the counter.
4. Receives the channel switch operation data and supplies it to TU-μP via the communications lines. TU-μP reads the tuning data of the channel commanded by T-μP from the channel list and converts it to a control voltage, then applies it to the tuner/IF circuit to select a channel. TU-μP also supplies the channel information to the internal channel controller in T-μP to change the channel indication on the digital multidisplay.
5. Receives the VTR operation mode from S-μP via the communications lines to drive the stop/pause/etc. indicators and informs the operator of the VTR operation state.
6. Receives the AUX select signal data during operating the channel up/down switch and controls the internal line/tuner switching memory output. This output is transmitted to TU-μP via the communications lines and is output from TU-μP to become the input select control signal for the audio/video processing circuit.
7. Inverts the internal VTR/TV switching memory output to ON/OFF alternately every time T-μP receives VTR/TV switch operation data. This output becomes the ON/OFF control signal for the RF converter circuit and the TV/VTR select control signal of the VHF output.
8. Detects the power frequency and a power failure data using the power frequency detection system. T-μP switches off the indicators and the indication in the digital multidisplay during a power failure to save power consumption of the μP and backs up the RAM storing the program data, tape counter data and channel data using a large capacitance capacitor for approx. 1 second, and at the same time, it increments the time using the built-in reference clock signal.

TU-μP: 1. Receives the IR remote function switch operation data and transmits it to S-μP via the communications lines, passing through T-μP. However, the remote channel up/down operation data, direct channel operation data and TV/VTR operation data are used in the μP. Receiving the data, S-μP determines the VTR operation mode and T-μP determines the channel.
2. Receives the line/tuner select data from the T-μP via the communications lines and outputs it to control the line/tuner input selection in the audio/video processing circuit.

2-2 Communications between μPs

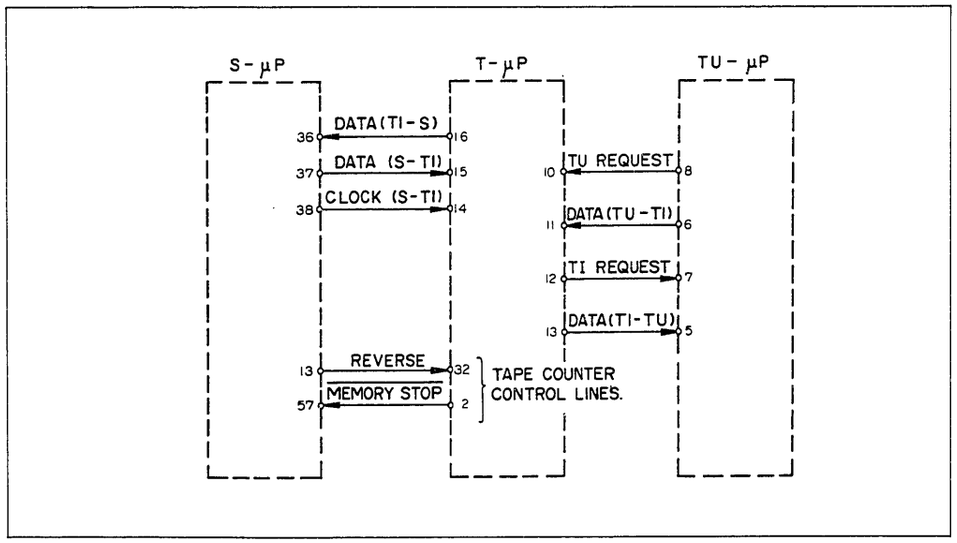


Fig. 2-2 Communications between μPs

As described previously, to fulfil the functions of the μPs, one μP needs the data in other μPs, so the μPs must always communicate with each other.
Fig. 2-2 shows the communications lines between the μPs. Communications between S-μP and T-μP are performed with a period of approx. 35ms. This is because T-μP must always know the operation data of S-μP which determines the VTR operation mode to inform the operator of the VTR's mode using LEDs and the digital multidisplay and also T-μP must transmit the operator's switch operation data detected by T-μP or TU-μP without a time lag.

S-μP and T-μP are connected via 3 communications lines (CLOCK (S-TI), DATA (S-TI), DATA (TI-S)) and 2 tape counter control lines (COUNT REV., $\overline{\text{MEMORY STOP}}$). The CLOCK (S-TI) signal is output from S-μP and synchronizes the data transfer between S-μP and T-μP. DATA (S-TI) and DATA (TI-S) are data buses; 8-bit serial data is transferred from S-μP to T-μP using DATA (S-TI) line and vice versa using DATA (TI-S) line. To match the phases of 8-bit serial data output from T-μP and S-μP, a header pulse is output when S-μP starts transmitting the 8-bit serial data (before the D0 bit is output). T-μP detects this header pulse at the rise of CLOCK (S-TI) signal. The phase of 8-bit serial data to be output by T-μP is matched with the phase of the header pulse. Fig. 2-3 shows the timing of these phases and Table 2-1 shows the 8-bit serial data output from S-μP and T-μP.

The tape counter control lines are provided to cancel the time lag between the tape counter in T-μP and S-μP. If S-μP and T-μP communicate the tape counter up/down count switching command and memory stop command, given to S-μP, via the communications lines, a time lag occurs causing counting errors and the tape stop position to drift when the memory stop function is used. Therefore, data must be communicated directly between S-μP and tape counter. The tape counter control lines consist of the "REVERSE" signal which determines the tape counter up/down count mode and the "MEMORY STOP" signal which gives the memory stop command to S-μP.

Data is communicated between T-μP and TU-μP when the remote function switch or channel switch is pressed by the operator and the channel is changed. T-μP and TU-μP are connected via 4 communications lines (DATA (TU-TI), DATA (TI-TU), TU REQUEST, TI REQUEST. DATA (TU-TI) and DATA (TI-TU) are 8-bit serial data communications lines. Data is transferred from TU-μP to T-μP via DATA (TU-TI) line and from T-μP to TU-μP via DATA (TI-TU) line, acknowledging the reception μP each bit. TI REQUEST and TU

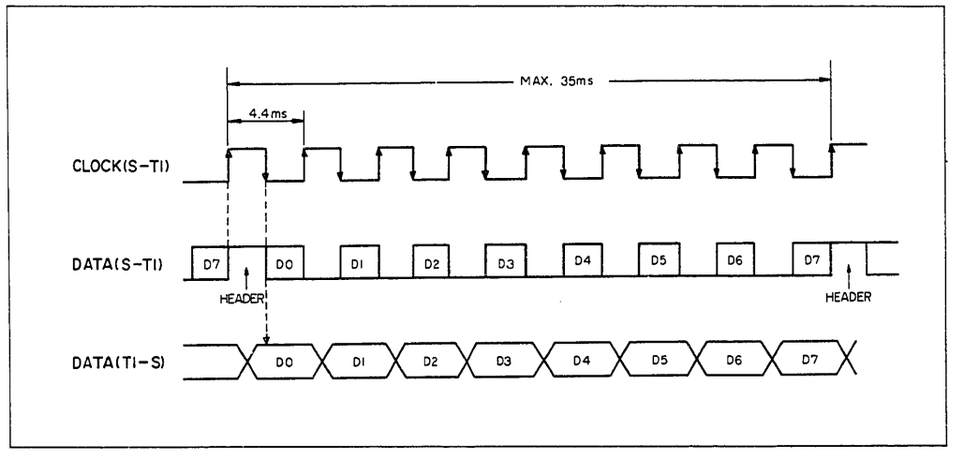


Fig. 2-3 Timing of Communications between S-μP and T-μP

REQUEST are the data transfer control signals output to TU-μP from T-μP and to T-μP from TU-μP respectively.
The transmission and reception μPs play the following roles.

Transmission μP	Reception μP
Requests data reception standby	
	Acknowledges data reception standby
Completes transfer data standby	
	Completes data reception

As described above, the transmission μP requests the reception μP to acknowledge and obtains acknowledgement from the reception μP. The transmission μP repeats this procedure twice for every bit. If the transmission μP cannot obtain acknowledgement from the reception μP within approx. 100 ms after it requests the reception μP to acknowledge, the transmission μP stops transmitting data and returns to the main loop.
Fig. 2-4 is a timing chart of data transfer between T-μP and TU-μP. Table 2-2 shows the 8-bit serial codes on the DATA (TI-TU) line and Table 2-3 the 8-bit serial codes on the DATA (TU-TI) line.

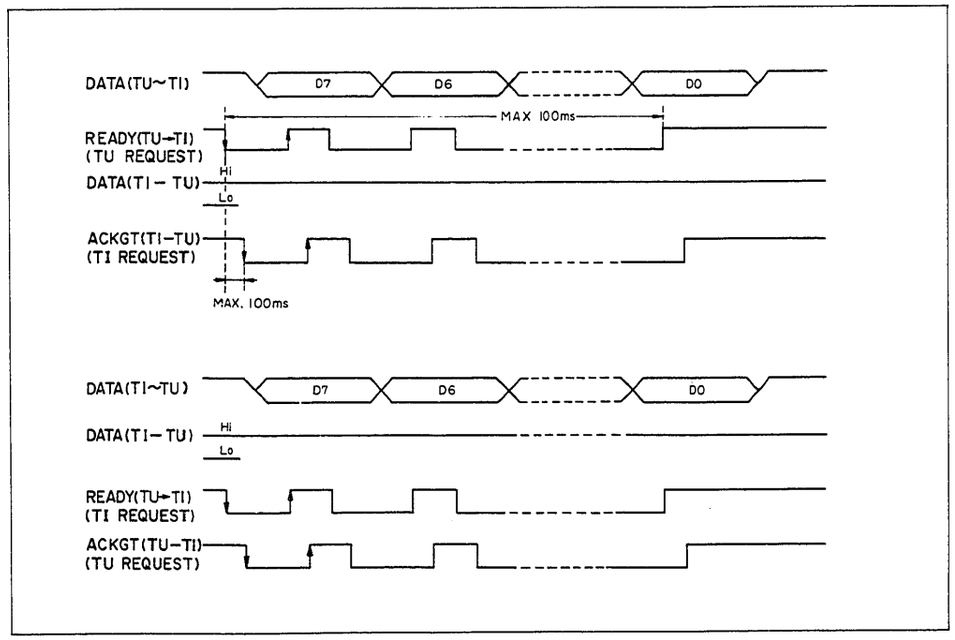


Fig. 2-4 Timing of Communications between T-μP and TU-μP

Table 2-1 Data (S-T) & Data (T-S)

	D3-D0 D7-D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Data (TI-S)	0	DIS-CNECT	PLAY	REC	RE-VERSE	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	A.DUB	V.DUB	PAUSE	EJECT	
	1	PROG.S TGL	PWR TGL	PWR ON	PWR OFF	T.STBY	TIME ON	COUNTER /REMAIN		KEY OFF				SS UP	SS DWN			
	2	SP	LP	EP	SAP	NO SAP	NO SAP											
	3																	
	4																	
	5																	
	6																	
	7																	
Data (S-TI)	0	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW	SEARCH	FWD SEARCH	REV	F.F	REW	STOP	REVERSE	V.DUB		SP	NO TAB
	1	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS		LP	PROG.S OFF
	2	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	REVERSE	V.DUB		EP	TAB
	3	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS			PROG.S OFF
	4	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	REVERSE	V.DUB		DEW SP	NO TAB
	5	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS		DEW LP	PROG.S ON
	6	POWER ON	PLAY	REC	A.DUB	F.ADV	SLOW		FWD SEARCH	REV SEARCH	F.F	REW	STOP	REVERSE	V.DUB		DEW EP	NO TAB
	7	POWER OFF	STILL	REC PAUS	A.DUB PAUS	PWR OFF				REPEAT			STOP PAUS		V.DUB PAUS			PROG.S ON

PROG.S : Program Search

Table 2-2 Data (TI-TU)

D3-D0 / D7-D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00 CH	01 CH	02 CH	03 CH	04 CH	05 CH	06 CH	07 CH	08 CH	09 CH						
1	10 CH	11 CH	12 CH	13 CH	14 CH	15 CH	16 CH	17 CH	18 CH	19 CH						
2	20 CH	21 CH	22 CH	23 CH	24 CH	25 CH	26 CH	27 CH	28 CH	29 CH						
3	30 CH	31 CH	32 CH	33 CH	34 CH	35 CH	36 CH	37 CH	38 CH	39 CH						
4	40 CH	41 CH	42 CH	43 CH	44 CH	45 CH	46 CH	47 CH	48 CH	49 CH						
5	50 CH	51 CH	52 CH	53 CH	54 CH	55 CH	56 CH	57 CH	58 CH	59 CH						
6	60 CH	61 CH	62 CH	62 CH	64 CH	65 CH	66 CH	67 CH	68 CH	69 CH						
7	70 CH	71 CH	72 CH	91 CH	92 CH	95 CH	96 CH	97 CH	98 CH	99 CH						
8																
9																
A	ST UP	ST DOWN									SC OFF	SC ON	TUNER LINE			
B																
C																
D			CH UP	CH DOWN		MUTE DISABL	MUTE ENABL	DISABLE	ENABLE							
E		KEY OFF														
F																

SC : Simulcast
ST : Slow Tracking

Table 2-3 Data (TU-T)

D3-D0 D7-D4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00 CH	01 CH	02 CH	03 CH	04 CH	05 CH	06 CH	07 CH	08 CH	09 CH				LOCK		
1	10 CH	11 CH	12 CH	13 CH	14 CH	15 CH	16 CH	17 CH	18 CH	19 CH			VHF(L)	VHF(H)	SUPER AFC OFF	UHF AFC ON
2	20 CH	21 CH	22 CH	23 CH	24 CH	25 CH	26 CH	27 CH	28 CH	29 CH						
3	30 CH	31 CH	32 CH	33 CH	34 CH	35 CH	36 CH	37 CH	38 CH	39 CH						
4	40 CH	41 CH	42 CH	43 CH	44 CH	45 CH	46 CH	47 CH	48 CH	49 CH						
5	50 CH	51 CH	52 CH	53 CH	54 CH	55 CH	56 CH	57 CH	58 CH	59 CH						
6	60 CH	61 CH	62 CH	63 CH	64 CH	65 CH	66 CH	67 CH	68 CH	69 CH						
7	70 CH	71 CH	72 CH	91 CH	92 CH	95 CH	96 CH	97 CH	98 CH	99 CH						
8																
9																
A																
B																
C				DISP OFF	POWER ON	POWER	DIGIT 9	DIGIT 8	DIGIT 7	DIGIT 6	DIGIT 5	DIGIT 4	DIGIT 3	DIGIT 2	DIGIT 1	DIGIT 0
D		CH UP		CH DOWN		POWER										F.ADV
E	STOP	KEY OFF	REWIND	F.FWD	R.SRCH	F.SRCH	STILL/ PAUSE		RECORD	CNT/ RMN	PLAY		AUDIO A/B	M.STOP SW		SLOW
F	R.SRCH	F.SRCH			ST UP	ST DOWN	PROG.			CLEAR	TV/VTR	PROG-S SW	V.DUB	A.DUB	SS UP	SS DOWN

SS : Slow Speed

2-3 Key Input

The key input circuit is an interface between the operator and each μP. The operator's commands are detected by the key matrix and IR receiver circuits and are supplied to the μPs to control the mechanism and circuits.

2-3-1 Key matrix circuit

Fig. 2-5 is a simplified diagram of the key matrix circuit of the switches on the front panel of the VTR. These switches, other than NORM/SELECT mode selector (S790), are of the push type and are input to T-μP and TU-μP via a matrix system.
T-μP uses 8 of the grid drive signals and one (Sh) of the segment drive signals which drive the digital multidisplay as key scan signals. There are 4 (MATRIX 0 -MATRIX 3) feedback input ports of the key scan signals. The matrix switch circuit detects 22 switch operations. The detected switch operation data is transmitted to S-μP and TU-μP via the circuits in T-μP and communications buses to trigger the functions of each μP.
TU-μP has 2 outputs ($\overline{\text{PHASE 0}}$, $\overline{\text{PHASE 1}}$) and 3 feedback input ports (MATRIX 0 - MATRIX 2) of the scan signals required by the matrix switch circuit. This matrix circuit detects 6 switch operations.

The detected switch operation data is transmitted to the tuning controller in the TU-μP to set the tuning data.

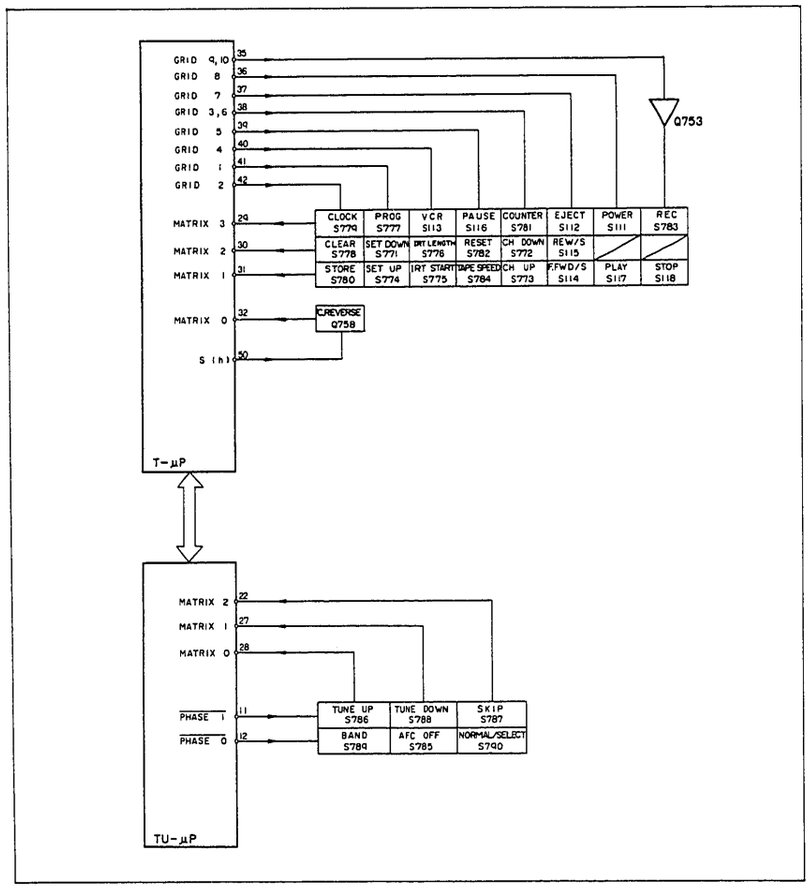


Fig. 2-5 Simplified Key Matrix Circuit Diagram

2-3-2 IR remote control system

The IR receiver circuit can receive the IR signals transmitted by the exclusive remote controller.
The exclusive remote controller has 9 switches (PLAY, RECORD, PAUSE, F. FWD, REWIND, STOP, POWER, CH-UP, CH-DOWN).
Fig. 2-6(a) is a simplified circuit diagram of the exclusive IR remote controller circuit.

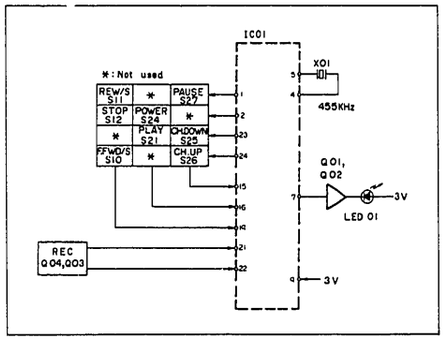


Fig. 2-6(a) Simplified IR Remote Controller Circuit Diagram

The μP in the remote controller detects switch operations via a matrix system and encodes the input into to the IR code, then pulse-pitch-modulates the code to generate a PPM signal. The μP modulates the 38kHz carrier signal using this PPM signal and outputs it to pulse-drive the LEDs.
Fig. 2-6(b) is a simplified diagram of the IR receiver circuit. This circuit consists of photodiode (PD1), IR AGC/detector/shaper IC (IR751), amplifier (Q756, Q757) and TU-μP.

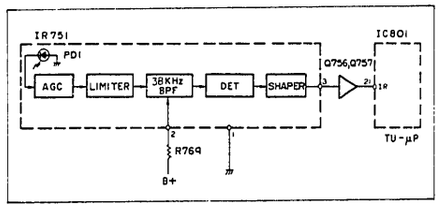


Fig. 2-6(b) Simplified IR Receiver Circuit Diagram

PD1: Receives the 38kHz IR signal transmitted from the IR remote controller via the infrared filter on the front of the VTR. The output voltage according to the strength of infrared signal is generated at the cathode of PD1.

IR751:
Consists of the AGC, limiter, 38kHz bandpass filter (BPF), detector and shaper.

AGC: Generates an error signal according to the strength of infrared signal to control the amplification and produces an IR signal of the constant output.

LIMITER:
Sets the amplitude of IR signal constant.

38kHz BPF:
Suppresses unnecessary signal components in the 38kHz IR signal. The center frequency of the BPF is determined by the resistance between pin 2 and B+.

DETECTOR:
Removes the 38kHz carrier components from the IR signal using an AM detection system to detect the PPM signal.

SHAPER:
Forms the wave of PPM signal to obtain a pulse with a steep ramp.

Q756/Q757:
Amplifies the PPM signal shaped and output from IR751 to an optimum input level for TU-μP.

TU-μP:
Decodes the PPM signal and transmits it to T-μP via the communications bus.

2-4 Mechanism/Circuit Control

When the μPs input operator's command via the key input circuit, the mechanism and circuits are set to the commanded mode. This operation is controlled by the mechanism/servo section and audio/video processing section.

2-4-1 Mechanism/servo control

General

Fig. 2-8 is a simplified diagram of the mechanism/servo control. S-μP mainly controls the whole mechanism and circuits and T-μP is concerned with partial control.

1. Cassette loading motor control:
Controls loading and ejection of a cassette.
2. Tape loading motor control:
Determines the mechanism operation modes - tape loading/unloading,

action/release of various brakes, backtension, take-up mechanism, etc.

3. Tape protection sensor monitoring:
   Detects abnormal operations in tape running using the dew, tape end and reel sensors.
4. Capstan motor control:
   Determines the tape speed and running direction, and fast forwards and rewinds the tape and takes up slack tape, etc.
5. Tape counter control:
   Makes T-μP count the pulses output by the HALL IC and calculates the amount of tape taken up to show it in the digital multidisplay. When the indication reaches "9999" in the fast forward and rewind modes, T-μP gives the stop command to S-μP.
6. Servo control:
   Determines the operation mode of the servo circuit. The servo circuit receives the feedback signals from the FG (Frequency Generator) and TACH pulse output from the cylinder and capstan motors and maintains the specified relationships between the speeds and phases (positions) of both motors.
7. Record safety tab detection:
   Detects the safety tab on the rear of a cassette to prevent the prerecorded programs from being erased by a mistake.

The above are the outline of mechanism/servo control. Next, the mechanism/servo control is described in details.

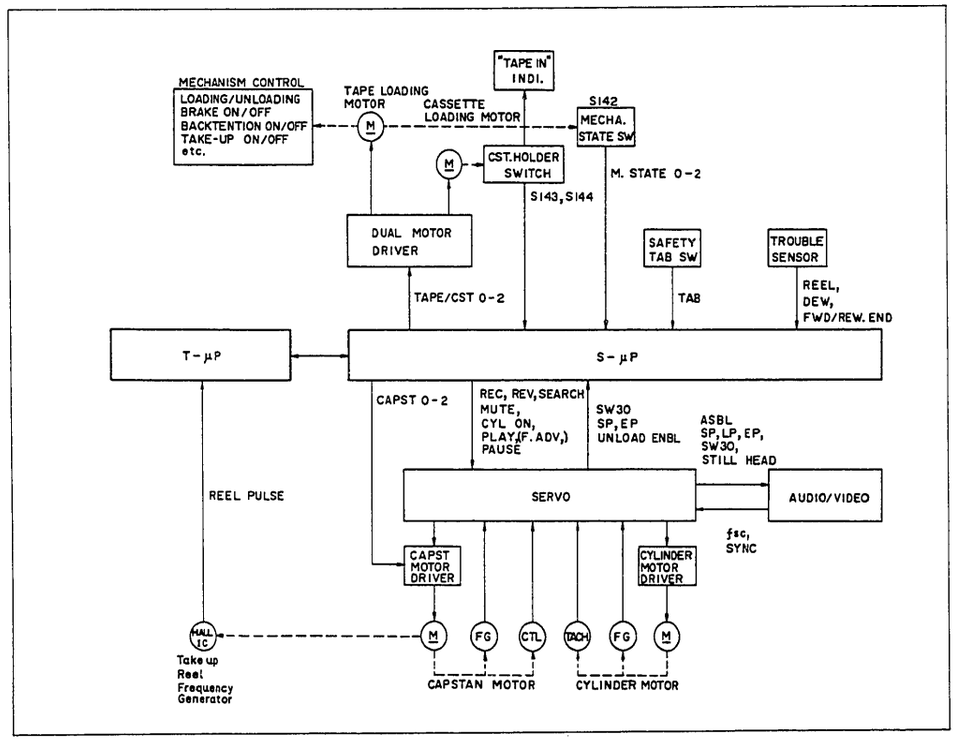


Fig. 2-8 Mechanism/Servo Control

Casstte/tape loading motor control

Fig. 2-9 is a simplified diagram of the cassette/tape loading motor control circuit. S-μP controls the rotation directions of both the cassette and tape loading motors using dual motor driver IC902 via 3 output lines. The rotation speeds are fixed and determined by the voltage (12V) applied to pin 9 of IC902. The driving periods of both motors are determined by the state sensor fed back from the respective objects of control. The driving period of the cassette loading motor is determined by two casstte holder state sensors S143/S144. The S143/S144 outputs also drive the "CASSETTE IN" indicator via cassette-in detector consisting of D910, D917. The driving period of the tape loading motor is determined by mechanism state sensor, S142.

Tape/mechanism protection

The cassette and tape loading motor control systems have protection devices which protect the tape, cassette, mechanism and motors when any abnormalities occur in the mechanism during loading or unloading. If the motor controller in S-μP cannot obtain the required state data from the controlled object when the loading or unloading operation period continues for more than 5 seconds for the cassette loading motor control system and more than 7 seconds for the tape loading motor control system, the controller reverses the motor rotation and returns it to the start position. If any abnormality occurs and it does not return to the start position, the controller shuts off the VTR power.

The protection device in the tape loading

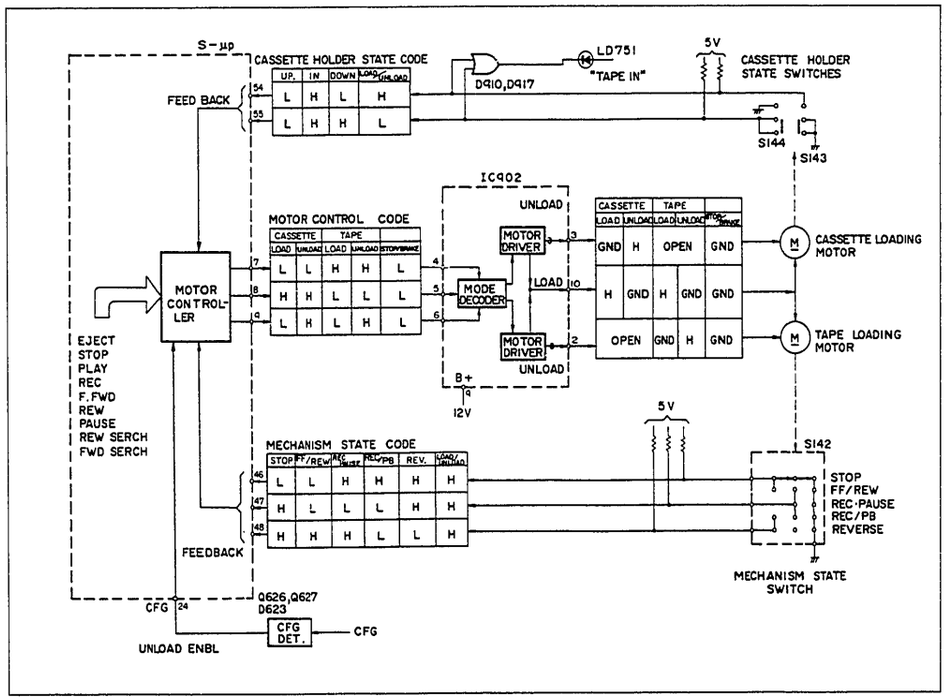


Fig. 2-9 Simplified Tape/Cassette Motor Control Diagram

motor control system also monitors whether slack tape is taken up normally by the supply reel during unloading. If unloading stopped with this tape take-up incomplete and the eject operation was done, the tape would be damaged. To prevent this, as soon as unloading starts, the rectified and inverted CFG signal (called "$\overline{\text{UNLOAD ENABLE}}$") is supplied through pin 24 of IC901 to the motor controller in S-μP from the servo circuit to monitor whether the capstan motor, the motive power to take up slack tape, rotates normally. When the CFG signal goes "Hi" during unloading, the unloading operation stops and the VTR enters the power off mode immediately.

Tape protection sensors

Fig. 2-11 is simplified diagram of the tape protection sensor circuit. This unit has 5 tape protection sensors - end sensors, reel lock sensor, cylinder lock sensor and dew sensor.

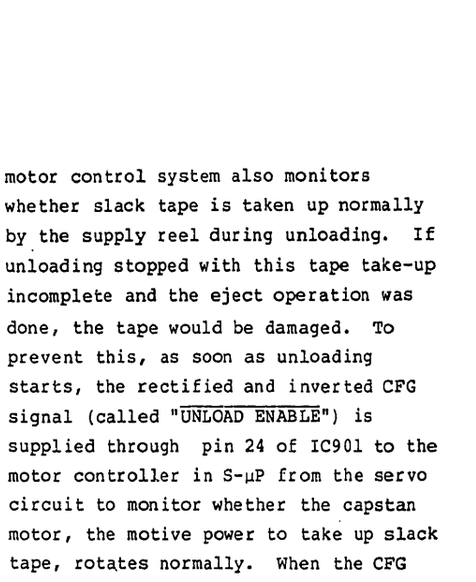


Fig. 2-11 Simplified Tape Protection Sensor Circuit Diagram

- End sensor:
  The take-up end sensor Q142 (supply end sensor Q141) receives light emitted by the end lamp through the tape leader at the reverse (forward) tape end and detects the tape end. When the forward end sensor receives light at the tape end in modes other than timer and IRT recording, it sets the VTR to the rewind mode automatically. When the rewind tape end sensor receives light, it sets the VTR to the stop mode automatically.
- Reel lock sensor:
  Detects the tape take-up condition and sets the VTR to the stop mode if any abnormalities occur. The rotation speed of the take-up reel disk is detected by the HALL IC, IC141, and the period of the HALL IC signal is calculated and the reel sensor detects any abnormality in the tape take-up operation.
  If the frequency is less than the values below in each mode, the tape take-up is abnormal.
  REC/PB/SEARCH: 6 sec.
  REW/F.FWD : 3 sec.
  However, this frequency detection is not performed in the pause mode.
- Cylinder lock sensor:
  Detects faulty tape winding onto the cylinder and abnormal rotation of the cylinder motor due to a motor fault and sets the VTR to the stop mode. Faulty rotation of the cylinder is detected by calculating the frequency of the head switching (SW30) signal. If the frequency is less than approx. 10Hz, it is judged that the cylinder speed is faulty.
- Dew sensor:
  Detects condensation in the VTR (especially on the cylinder) during Power ON and flashes the stop indicator while dew is present to warn the operator; at the same time, it inhibits any function switch inputs. Condensation is detected when the dew sensor, the resistance of which changes low when condensation occurs, increases the voltage drop across resistor R932.

Capstan motor control

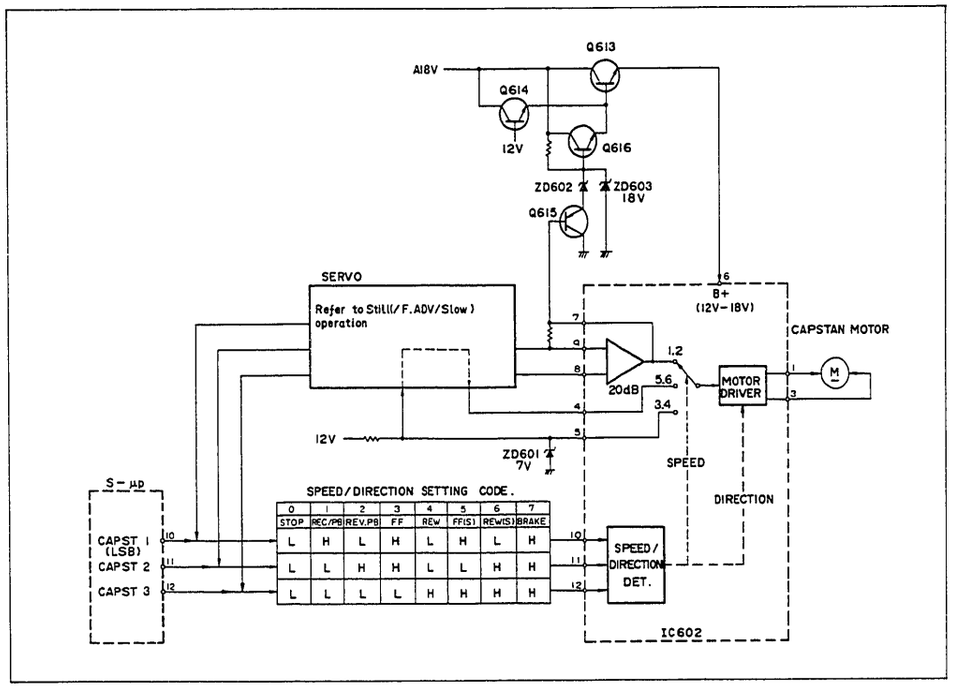


Fig. 2-12 Simplified Capstan Motor Control Circuit Diagram

The capstan motor keeps the tape speed constant in the record and playback modes and takes up the tape onto the take-up or supply reel in the fast forward, rewind, (frame advance) and unloading modes. Fig. 2-12 is a simplified diagram of the capstan motor control circuit. To perform the above controls, S-μP determines the motor speed and rotation direction using capstan motor driver IC602. The power supply voltage applied to IC602 pin 6 is adjusted to an optimum value from a minimum of 12V to a maximum of 18V due to its load by the variable power supply circuit consisting of Q613 - Q616, ZD602 and ZD603 to reduce motor's power consumption. The variable power supply circuit output is derived from the emitter of Q613. Two output voltage limiting voltages and a variable voltage are applied to Q613's base to control the output voltage of the variable power supply circuit. One limiting voltage maintains the output voltage at more than 12V using Q614. The other limiting voltage maintains the output voltage at

less than 18V using ZD603. The latter limiting voltage is produced by adding the terminal voltage (17V) of ZD602 to the voltage obtained by amplifying the capstan drive voltage in the servo system by approx. 20 dB through Q615. Since this voltage is controlled so it is proportional to the load, the output voltage follows it.
S-μP transmits 3-bit capstan speed/direction setting codes to IC602. (However, the control codes are supplied from the servo circuit in the frame advance mode.) IC602 decodes them to determine the motor's speed and rotation direction. The motor speed is determined by the voltages applied to the 3 speed setting inputs of IC602 as shown in the table below.

Speed setting pins of IC602	Voltage	Selected codes
8 and 9	0 - 5V (Variable)	1 (001) or 2 (010) *1
4	9V: Speed up (9V: SP 6V: $\overline{SP}$) 5V: Speed down (5V: SP 4V: $\overline{SP}$ 4V: Normal	5 (101) or 6 (110) *2
5	7V	3 (011) or 4 (100)

*1: The capstan drive voltage from the servo circuit is applied and is amplified in the IC by 20 dB, then it is supplied to the motor driver in IC602.

*2: The supply voltage and mode are determined by the servo circuit. Normally, 4V is applied. In the frame advance or slow motion mode, the speed up voltage (9-6V) or speed down voltage (5-4V) is selected and applied to pin 4. In this mode, the servo circuit sets IC602 to the "FF(S)" or "REW(S)" mode and makes IC602 select the voltage applied to pin 4. (See the servo circuit for details.)

The rotation direction is determined by selecting the output ports of the motor driver in IC602 according to the capstan speed/direction setting codes. When the LSB of the capstan speed/direction setting codes is "Lo" (excluding the stop mode), the reverse mode is selected and the motor drive current flows from pin 3 to pin 1. When the LSB is "Hi" (excluding when braked), the forward mode is selected and the motor drive current flows from pin 1 to pin 3. The 2 output ports are set open in the stop mode, and when braking is applied, the output ports are short-circuited.

Tape counter control

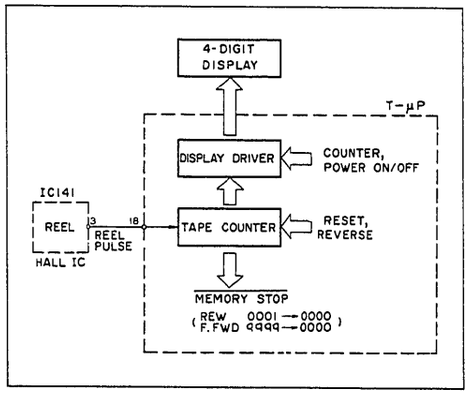


Fig. 2-13 Simplified Tape Counter Circuit Diagram

Fig. 2-13 is a simplified diagram of the tape counter control circuit. The tape counter in T-μP counts the reel pulses generated by the take-up reel disk rotation and indicates them in the digital multidisplay by 4 digits. The reel pulse is derived from HALL IC (IC141). The HALL IC detects the change in magnetic flux caused by the rotation of the magnet magnetized in 8 poles on the take-up reel disk and generates 4 cycles of square wave when the disk rotates by one turn. T-μP determines the counter mode so the counter counts up when the "REVERSE" signal described in "Communications between μPs" is "Lo" and the counter counts down when the signal is "Hi", and counts the reel pulses. The count data is transmitted to the display driver. When the counter display mode is commanded by the operator, the 4-digit clock/counter display in the digital multidisplay is switched to the counter display mode from the clock display mode and the count data is displayed. When the power is turned off from on in the counter display mode, the display is automatically switched to the clock. When the power is turned on again, the counter display is restored. When the reset is commanded by the operator, the counter is reset to 0. The tape counter has a memory stop function. When the digital multidisplay is in the counter display mode and the counter reaches "9999" during rewind or "0000" during fast forward, the memory stop signal (Pulse width: 400ms) is generated and supplied to S-μP via the "MEMORY STOP" line described in "Communications between μPs". When S-μP receives the "MEMORY STOP" signal in the fast forward or rewind mode, it sets the VTR to the stop mode.

Servo Circuit Control

Fig. 2-14 shows the control lines between the servo circuit and S-μP and between the servo circuit and audio/video processing circuit. S-μP and the servo circuit are connected via 10 outputs REC, PLAY, SEARCH, (F. ADV), PAUSE, REVERSE, MUTE, $\overline{CYL\ ON}$, $\overline{SP\ SW}$, $\overline{EP\ SW}$ and 4 inputs SP, EP, CYL LOCK, UNLOAD ENBL (CFG).

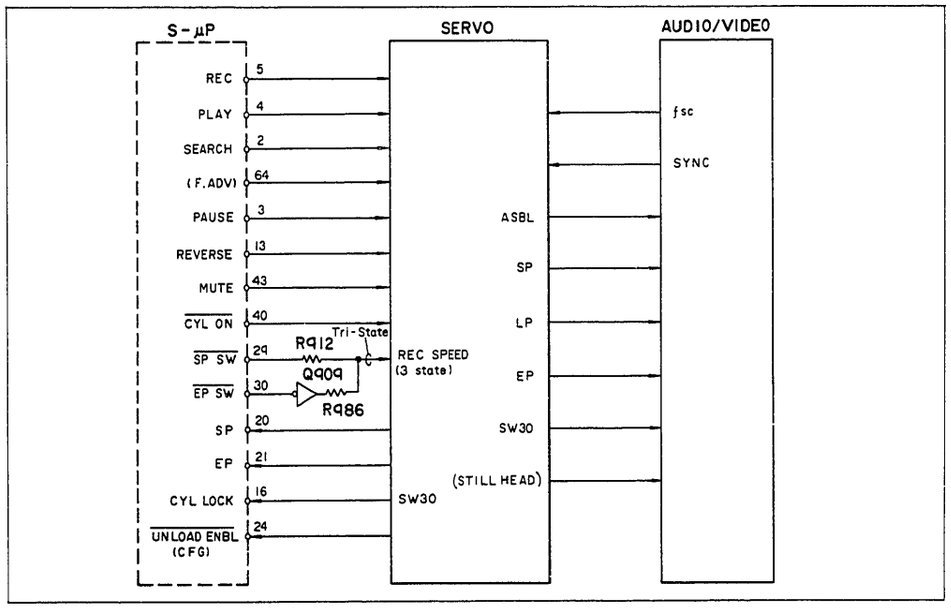


Fig. 2-14 Servo Circuit Control

- The outputs - "REC, PLAY, SEARCH, (F.ADV), PAUSE, REVERSE" - determine the operation mode of the servo circuit.
- The output, "MUTE", determines the control pulse recording inhibit period during loading and recording pause.
- The output, "$\overline{\text{CYL ON}}$", operates the cylinder servo.
- The outputs, "$\overline{\text{SP SW}}$" and "$\overline{\text{EP SW}}$", determine the recording tape speed. Using both outputs, the tristate voltage (SP: 0V, LP: 2.5V, EP: 3.8V) is produced and supplied to the servo circuit.
- The inputs, "SP" and "EP", receive the tape speed data necessary for the tape speed to be indicated in the digital multidisplay.
- Inputs, "CYL LOCK" and "UNLOAD $\overline{\text{ENBL}}$"(CFG), are trouble sensors described in "Tape protection sensor".

The servo circuit and audio/video processing circuit are connected via 6 outputs (ASBL, SP, LP, EP, SW30, STILL HEAD) and 2 inputs (fsc, SYNC).

- The output, "ASBL", inhibits recording of audio/video signals for approx. 0.7 seconds just after recording pause is released to optimize tracking.
- The outputs, "SP, LP, EP", determine the emphasis/deemphasis of the audio/video signals during recording and play.
- The output, "SW30", switches the playback outputs of 2 video heads to a continuous signal, changes the phase shifting direction of the chroma signal for every channel and shifts the carrier frequency used for the luminance signal modulation by fH/2 for every channel.
- The output, "STILL HEAD", selects the video head exclusive for still play in the still mode.
- The input, "fsc", produces the clock signal necessary in the digital servo system.
- The input, "SYNC", synchronizes the cylinder servo during recording with the vertical sync signal in the incoming video signal.

The servo circuit operation will be described later in detail.

2-5 Digital Multidisplay/Mode Indicator Control

The VTR uses LEDs and a digital multidisplay to inform the operator whether the VTR is operated as commanded by the operator and warn the operator of the abnormal operations of the VTR. The LEDs and digital multidisplay are driven by T-μP.

Fig. 2-15 shows the connections between T-μP and the LEDs and digital multidisplay. The LEDs are directly driven by T-μP and display 7 operation modes (STOP/DEW WARNING, PAUSE, VTR, PLAY, REC, F.FWD and REW). All the indicators except "VTR" are controlled by the operation mode data supplied from S-μP and the "VTR" indicator is controlled by the TV/VTR memory output of T-μP.

The digital multidisplay is driven by the dynamic drive system and indicates the following 8 items.

1. Input signal (AUX)
2. Channel
3. Tape speed
4. Tape counter
5. Clock
6. Program
7. IRT start/length/remaining time

Concerning items 1 - 3 above, exclusive segments are provided in the digital multidisplay. For the remaining items 4 - 7, one item is selected by the operator and is displayed. Fig. 2-16 shows the locations of the grids and segments in the digital multidisplay. Table 2-5 shows the relation of grids and segments with respect to the displayed contents.

T-μP receives the display data and display select data from the internal circuits and S-μP to control the display. When a power failure occurs (detected by the power failure signal), all displays go off to reduce the backup power consumption. When the power is turned off, only the clock is displayed.

When the power is turned on, only the operation mode which was selected by the operator is displayed. To drive the digital multidisplay dynamically, T-μP outputs 8-phase grid drive pulses (GRID 1 - GRID 10) with 60Hz and duty cycle 9% and 9 segment drive pulses (Sa - Si). To prevent flickering caused by the difference between the power frequency of the heater in the display and the grid lighting frequency, the frequency of grid drive pulses is synchronized with the heater power frequency (60Hz) input from pin 19.

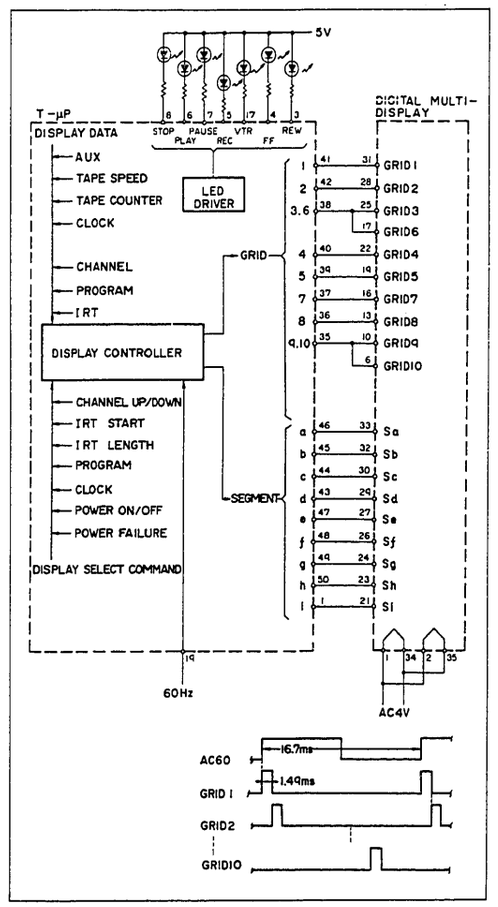


Fig. 2-15 Simplified Digital Multidisplay/ Indicator Control Diagram

Table 2-5 Grid/Segment Matrix

GRID / SEGMENT	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1
a	SP		a	a	:	a	a		a	a
b		AUX	b	b	3	b	b		b	b
c		TIMER	c	c		c	c		c	c
d		PROG	d	d		d	d	CH	d	d
e	LP		e	e		e	e	IRT	e	e
f	SLP		f	f		f	f	PM	f	f
g		ON	g	g		g	g	AM	g	g
h		OFF	1	2		4	WKL	WED		AFC
i		1W	2W	SUN		MON	TUE	THU	FRI	SAT

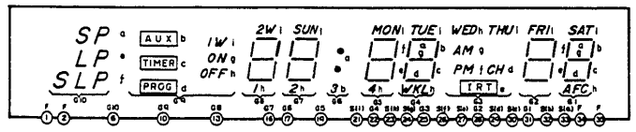


Fig. 2-16 Grid/Segment Location

2-6 Clock/Timer/IRT Control

The VT-1100A/1105A have timer recording and instant recording timer (IRT) functions. When the operator inputs required TV programs and the times using these functions, recording starts automatically when the preset time is reached and the VTR power is turned off or it enters the timer standby mode when the recording stops.
The timer can preset 2 TV programs in 2 weeks including weekly or daily programs. The IRT has a simplified program setting function which is able to timer-record one program.

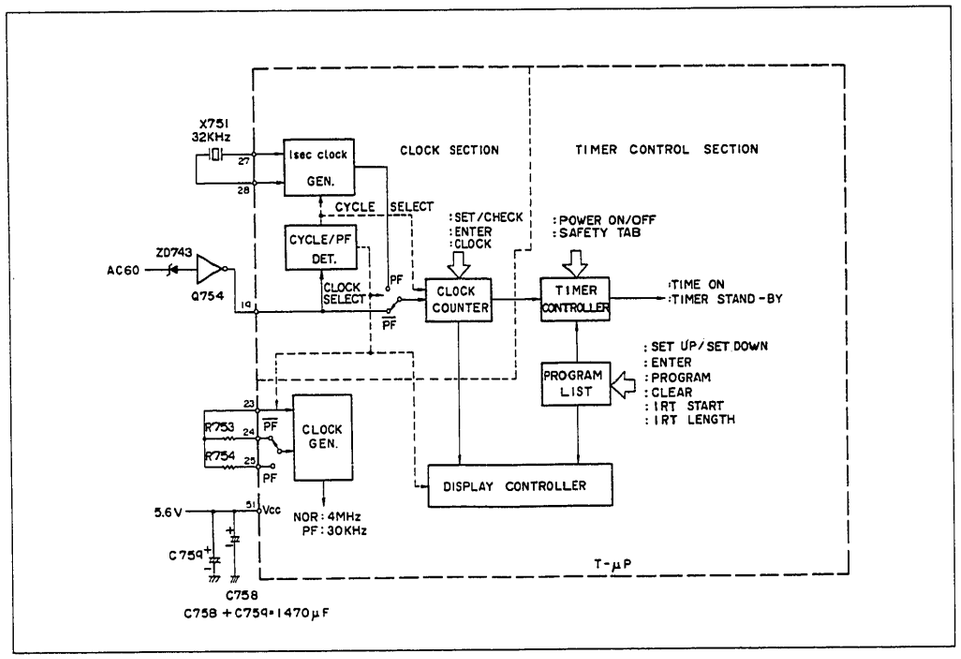


Fig. 2-17 Simplified Clock/Timer/IRT Control Diagram

Fig. 2-17 is a simplified diagram of the clock/timer/IRT control circuit in T-μP. The power input, pin 51, of T-μP receives the 5V source from the power supply circuit normally and from the large-capacitance capacitor C759 during a power failure. When a power failure occurs, the latter power supply maintains the present time and input data in the program list for approx. 1 second. The clock/timer/IRT control is realized by the clock section determining the time, the timer control section determining the timer output and the program list storing the required TV-program data.
The clock section consists of the clock counter, 1 sec clock generator and power cycle/failure detector.

Clock Counter:
Counts the power frequency input from pin 19 via inverter Q754 in the normal mode and the frequency output from the REF 50/60 generator in T-μP during a power failure to determine the time and date. The determined time and date are indicated in the digital multidisplay via the display controller. The time is corrected when the data in the clock counter is modified by operating the CLOCK, ENTER and SET keys which are input via the key matrix circuit.

1 sec Clock Generator:
When a power failure occurs, the clock (power frequency) signal is not supplied to the clock counter. This generator generates a signal the frequency of which is near the frequency of the clock signal which has been supplied before a power failure and supplies it to the clock counter. The 1 sec clock generator generates the frequency determined by the resonance frequency of the quartz crystal connected to pins 27 and 28 and counts it down to the power frequency detected by the power cycle/failure detector.

Power Cycle/Failure Detector:
Always detects the frequency and supply state (power failure) of the AC power supply input via pin 19. When the power frequency period is less than 18.3 ms, the detector detects that the power frequency is 60Hz, and when the period is between 18.3 and 50 ms, it detects 50Hz, and when the period is 50 ms or more, it detects a power failure.

When receiving the power frequency detection output, the power cycle/failure detector controls the following 2 items:

1. Determines the division ratio so the output frequency of the 1 sec clock generator is equal to the power frequency before a power failure occurs.
2. Determines the preset data in the clock counter to correct the counting difference between power frequencies of 50Hz and 60Hz.

When receiving the power failure detection output, the power cycle/failure detector controls the following 3 items:

1. Selects the clock signal applied to the clock counter. It selects the power frequency input at pin 19 normally and selects the 1 sec clock generator output during a power failure.
2. Opens all input ports to reduce consumed power of T-μP during a power failure. This switches off the indicators and digital multidisplay.
3. Switches the μP's system clock frequency to reduce the consumed power of the μP. It selects resistor R753 connected to pin 24 normally to switch the system clock frequency to 4MHz and selects R754 connected to pin 25 during a power failure to switch the frequency to 30kHz.

The timer controller section uses the data (time and date) output from the clock counter section, data in the program list described later and the operation mode data from S-μP, and determines the command codes applied to S-μP.
When a program is set and the power switch of the VTR is turned off, T-μP transmits the "TIMER STAB" code to S-μP to set the VTR to the timer standby mode. When a cassette without its safety tab is loaded and the timer standby code is applied to the S-μP, the S-μP ejects the cassette immediately and the T-μP flashes "TIMER" in the digital multidisplay to warn the operator.
When the "TIME ON" time is reached, T-μP transmits the "TIME ON" code to S-μP.

When receiving this code, S-μP transmits the "REC" code to T-μP. During the TIME ON period, T-μP controls the TIME ON code output so the operation mode data sent from S-μP is always "REC". However, T-μP interrupts the timer recording when condensation (dew) occurs or the tape end is detected.

The program list stores the input data - times and dates of programs for timer recordings and the time (length) of IRT program, etc. Table 2-6 shows the data stored in the program list.

TIMER PROGRAM LIST				
PROG. NO.	CHANNEL	DAY	TIME ON	TIME OFF
1				
2				
3				
4				
IRT PROGRAM LIST				
CHANNEL	TIME ON		LENGTH	

Table 2-6

The above data is input by operating 9 keys (SET UP, SET DOWN, STORE, PROGRAM, CLEAR, IRT START, IRT LENGTH, CHANNEL UP, CHANNEL DOWN) as described in "Key Input". The programming procedure is as follows.
When the "PROG." key is pressed, the digital multidisplay enters the program display mode and the program No. can be selected and input. The program No. is selected by pressing the "SET UP/DOWN" key. Pressing the "STORE" key enables the channel, day, time ON and time OFF to be input in sequence in the determined program No. line. The setting procedure is that the "SET UP/DOWN" key is pressed to select the input data, then the "STORE" key is pressed to store the data in the designated line in the program list. Data input of one program is completed in this way and is followed by the data input procedure of the next program.
When the necessary data input is completed, the program Nos. (1, 2 or W) light from flashing.
The input data of each program No. is deleted when the timer recording of the program is completed or the "CLEAR" key is pressed after recalling the program No. However, the input data of the weekly or daily program is erased only when the "CLEAR" key is pressed.

IRT Control

Instant recording timer (IRT) is timer recording with the simplified program setting procedure. The recording start time can be set within a maximum of 24 hours from the present time at 30-minute or 1-hour intervals. The recording end time is determined automatically by selecting 6 recording length times (30, 60, 90, 120, 180, 240 minutes). When a recording length time is selected without setting the recording start time, the present time is set automatically for the start time and recording starts immediately.
To release IRT, set the recording length time to display "0:00" and then wait for 8 seconds. The above times can be set only when the VTR power is turned on. The remaining time to be recorded is indicated in the digital multidisplay during IRT. When the display reaches "0:00", the VTR power is turned off.

3. SERVO

3-1 General

The servo system in the VTR is divided into three loops according to the objects of control - the cylinder servo controlling the rotating video heads, the capstan servo controlling the video tracks and the tension servo.

The tension servo loop maintains the tape tension constant; it keeps the compression strength of tape against the video heads in the optimum condition so a stable RF signal is produced during recording and playback. The tension servo operation is performed entirely mechanically.

Fig. 3-1 is a simplified cylinder and capstan servo operation diagram. The cylinder servo loop controls the phase and speed of the cylinder motor in the video head assembly; it determines the position of vertical sync signal on the video tape to satisfy the specified format (VHS magnetic tape pattern in the VHS system) and suppresses the time axis fluctuations of video signal to become minimum.

The capstan servo loop controls the phase and speed of the capstan motor in the capstan assembly so the video heads can trace (play back) the recorded video tracks correctly.

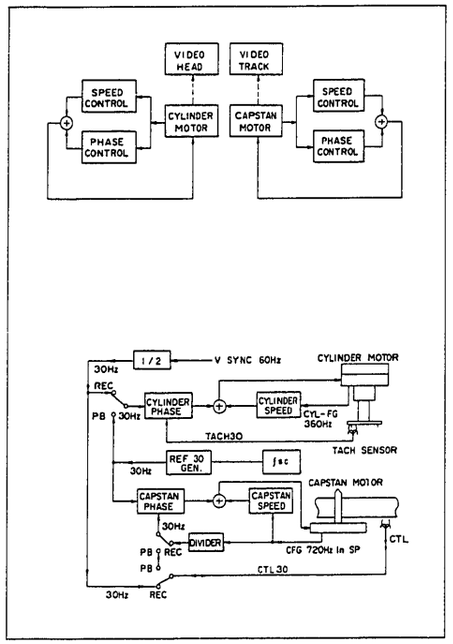


Fig. 3-1 Cylinder/Capstan Control

Recording Cylinder Servo

From the composite video signal supplied from a TV or video camera, only V. SYNC (60Hz) is derived by the video circuit in the VTR and is divided by two to become SYNC 30. Using this SYNC 30 as a reference signal and the TACH signal as a comparison signal, the cylinder servo loop compares the phases of both signals and generates an error voltage according to the phase difference.
The cylinder servo loop detects the period of CYL-FG pulses of which the frequency is 360Hz with respect to 30 rotations of the cylinder and generates an error voltage according to the rotation speed error (wow & flutter).

The cylinder servo loop feeds back both error voltages negatively to the cylinder to control the speed and phase of the cylinder.

Recording Capstan Servo

The capstan servo loop must run the tape smoothly at an accurate speed to record the SYNC 30 signal correctly on the bottom track of the tape without time fluctuations. To do this, the capstan servo loop detects the period of CFG pulses (720Hz in SP) to control the speed. To control the phase, the capstan servo loop compares REF30Hz produced by the crystal oscillator in the VTR and 30Hz obtained by dividing the CFG frequency and uses the resultant signal.

The tape speed during recording can be set by operating the tape speed select switch.

Playback Cylinder Servo

The playback cylinder servo operates in the same way as the recording cylinder servo except that it changes the reference signal from SYNC 30 to REF30Hz produced by the crystal oscillator.

Playback Capstan Servo

The capstan servo loop uses the CTL pulse (30Hz) played back by the CTL head as the comparison signal for the phase control circuit during playback. This is greatly different from the recording capstan servo and the important point in the playback capstan servo. The playback capstan servo compares the phases of REF30Hz and CTL30Hz on the tape to control the tape transport. The speed control loop is the same as in recording.

Since the tape speed is automatically detected and switched when a recorded tape is running, the tape speed select switch on the front panel is not concerned with tape speed switching during the PB mode.

The tracking is optimized by shifting the phase of the capstan.

Servo Control Signals

As described previously, the servo system handles different signals in each mode. The signals are collected and listed below.

Cylinder Servo

System	Mode	Reference Signal	Waveform	Comparison Signal	Waveform
Cylinder Phase Control	Recording	SYNC30Hz	Sample pulse	TACH30	Digital trapezoid
	Playback	REF30Hz		TACH30	
Cylinder Speed Control	Recording	CYL-FG 360Hz	Sample pulse	CYL-FG 360 Hz	Digital sawtooth
	Playback	CYL-FG 360Hz		CYL-FG 360 Hz	

Capstan Servo

System	Mode	Reference Signal	Waveform	Comparison Signal	Waveform
Capstan Phase Control	Recording	REF30Hz	Digital trapezoid	CFG30 *2	Sample pulse
	Playback	REF30Hz		CTL30	
Capstan Speed Control	Recording	CFG *1	Sample	CFG *1	Digital sawtooth
	Playback	CFG *1		CFG *1	

*1: The frequency of CFG pulse is varied in various conditions as follow.
1. SP: 720Hz
2. LP: 360Hz
3. EP: 240Hz
4. SEARCH: 2160Hz

*2: CFG30 is produced by dividing the above CFG to 30Hz.

3-2 Servo Circuit

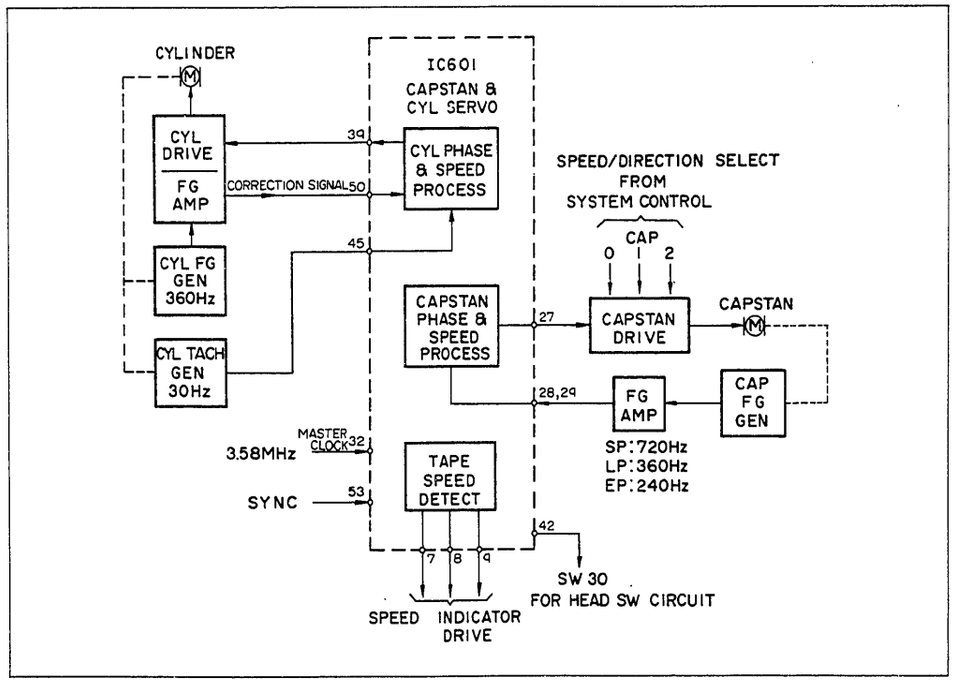


Fig. 3-2 Servo Block Diagram

Fig. 3-2 is a block diagram of the servo circuit. The cylinder drive signal leaves IC601 at pin 39 from which it is applied to the cylinder drive FG amplifier circuit. This cylinder drive IC applies the drive signal to the cylinder motor and amplifies the FG signal. As the cylinder rotates, it is mechanically coupled to both the cylinder FG generator and cylinder tach generator. These two signals are used as the feedback and comparison signals in cylinder motor servo loops. The cylinder FG (frequency generator) signal is 360 Hz and is applied to the FG amplifier in the cylinder drive IC. A correction signal is generated by the FG generator and applied to pin 50 of IC601, the capstan and cylinder servo processing IC.

The capstan motor drive signal generated by IC601 is supplied from pin 27 to the capstan drive circuit. The capstan drive circuit also receives speed control signals from the system control μP. The capstan control signals are necessary to allow different modes of operation SP, LP, and EP, and fast foward, rewind, and search. As the capstan motor rotates, it is electromechanically coupled to the capstan FG generator which generates a 720Hz signal in the SP mode, 360Hz in LP, 240Hz in EP and 2160Hz during forward and reverse search. The capstan FG signal is then passed through an FG amplifier and applied to pins 28 and 29 of IC601.

During playback, the speed detection circuit in IC601 determines the playback speed. Pins 7, 8 and 9 provide this information to the system control circuit and drive the speed indicator in the digital multidisplay.

Capstan and cylinder servo IC601 also receives a 3.58 MHz signal at pin 32 from the signal processing circuit. The 3.58 MHz signal is used in the IC as a master clock to synchronize the operation of the servo loops. A composite sync is also applied to pin 53; this provides synchronization during various modes of operation. The 30Hz signal used in the head switching circuit is supplied from pin 42 of the capstan/cylinder servo IC601.

3-3 Capstan and Cylinder Servo Processing

3-3-1 General

Fig. 3-3 is a block diagram of the main servo processing IC. Digital counters are utilized extensively within the IC for the speed and phase loops of both cylinder and capstan. The digital counters detect speed and phase errors and generate the correction signals. Earlier servo systems utilized a combination of both digital and analog circuits in order to generate trapezoid correction waveforms. The digital capstan and cylinder servo processing IC, IC601, does not generate these waveforms internally. Instead, the correction signal generated by the digital counter is utilized to control the duty cycle of a pulse width modulated circuit to develop the capstan and cylinder drive signals.

The CYL-FG signal is applied to pin 50. The cylinder FG signal is used as a comparison signal in the cylinder speed loop. The tach signal is applied to pins 4 and 5 of IC601, peak-detected, a positive tach pulse is selected and is applied to the tach shift monostable multivibrator (MM) which supplies the delayed tach signal to both the cylinder phase loop and the switching 30Hz generator. The switching 30Hz generator in IC601 supplies a head switching 30Hz signal from pin 42. The cylinder phase loop utilizes the delayed tach signal provided by the tach shift MM as a comparison signal. The delayed tach signal is compared to the composite sync information at pin 53 during recording and the reference 30Hz generator output during playback. The reference 30Hz signal is generated by dividing down the 3.58MHz supplied to pin 32. During playback, the output from the reference 30Hz generator (30Hz) is applied to the capstan phase error detector via the tracking MM. During recording, vertical sync information is supplied to the record control track generator. The record control pulse is supplied from pins 59 and 60 to the control track head.

The cylinder speed error PWM signal from pin 43 is passed through a lowpass filter to pin 41. The cylinder phase error PWM

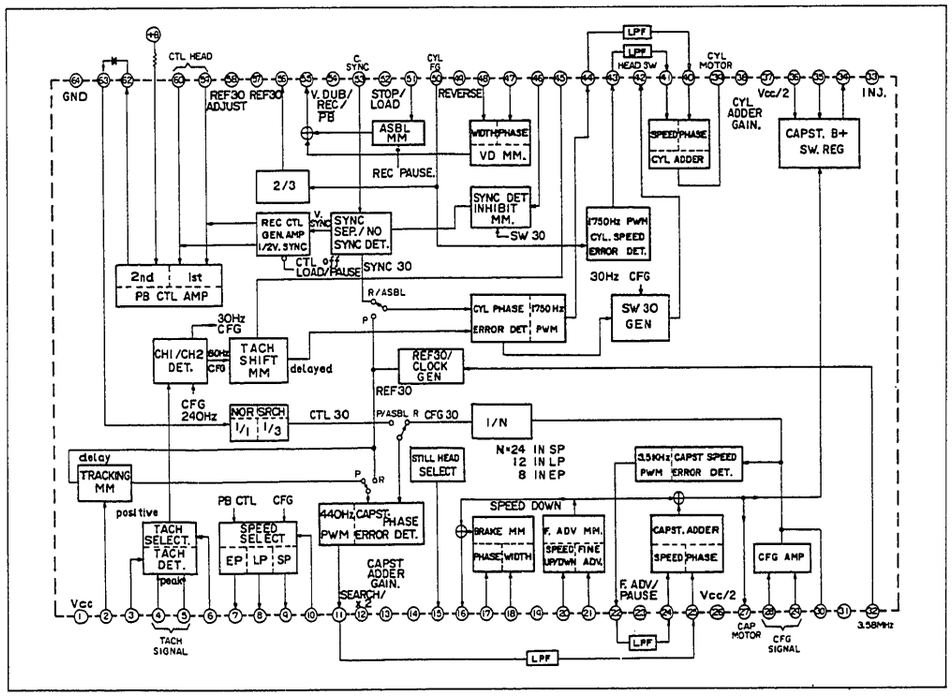


Fig. 3-3 Detailed Main Servo Processing IC Block Diagram

signal from pin 44 is supplied through another lowpass filter to pin 40. The cylinder speed and phase error signals from pins 41 and 40 respectively are applied to an adder circuit to develop the cylinder drive signal at pin 39.

The capstan phase and speed loops are similar to those of the cylinder. The frequency of the capstan FG signal (CFG) depends upon the mode of operation. The CFG signal is applied from pins 28 and 29 of IC601 to the capstan speed loop and capstan FG 30Hz generator circuits. The capstan FG signal is compared to an internal reference value in the capstan speed loop generating the speed error PWM signal at pin 22. The capstan FG signal frequency is 720 Hz for SP, 360 Hz for LP, and 240 Hz for EP. The capstan FG 30 (CFG) generator consists of a programmable divider which develops a 30Hz output signal. During the SP mode, the FG signal is divided by 24, in LP, by 12 and in EP, by 8. During recording the CFG 30 signal is used as the comparison signal in the capstan phase loop. During playback, a 30Hz comparison signal is generated from the playback control track pulse (CTL) which is applied at pins 59 and 60. The CTL pulse is amplified by the 1st and 2nd amplifiers in IC601 and is output from pin 62. The amplified CTL pulse at pin 62 is reapplied through pin 63 to the CTL divider in IC601. The CTL divider consists of a programmable divider which develops a 30Hz output signal. In modes other than search, the CTL signal is directly applied to the capstan phase loop for comparison. The CTL signal is divided by 3 during search.

A reference signal for the capstan phase loop during playback is supplied by the tracking MM. The tracking MM adjusts the delay of the reference 30Hz from the reference 30Hz generator. During recording, the reference signal for capstan phase is applied directly from the reference 30Hz generator. The capstan phase error PWM signal leaves IC601, pin 11, and is applied through a lowpass filter to pin 25. The speed error PWM signal from the capstan speed loop is applied to a lowpass filter from pin 22 and is fed back into the IC via pin 24. The capstan speed and phase error signals from pins 24 and 25 are applied to an adder circuit to generate the capstan drive signal at pin 27.

3-3-2 Cylinder processing

Fig. 3-4 is a simplified diagram of the cylinder speed control circuit. The cylinder FG signal (360Hz), amplified by motor driver/amplifier IC1651, is applied to pin 50 of IC601. Then the cylinder FG signal is applied to the cylinder speed error detection circuit. The cylinder speed error detection circuit consists of three digital counters which generate the digital speed error signal. A 1.8MHz (fsc/2) clock signal which is generated from the counted down 3.58MHz signal determines the speed at which the counters operate and is applied to the cylinder error detect circuit. The cylinder speed must be varied slightly during still, forward and reverse search modes. The STILL, SEARCH and REVERSE commands are applied to pins 23, 12 and 49 respectively. The cylinder speed error detection circuit also supplies a control signal to the cylinder phase loop to turn it on and off. The digital speed error signal generated by the cylinder speed error detection circuit is applied to the speed PWM which operates at a frequency of 1750Hz. The digital speed error signal controls the duty cycle (or "on" time) of the speed PWM circuit. The detail operation of the cylinder speed loop is described later.

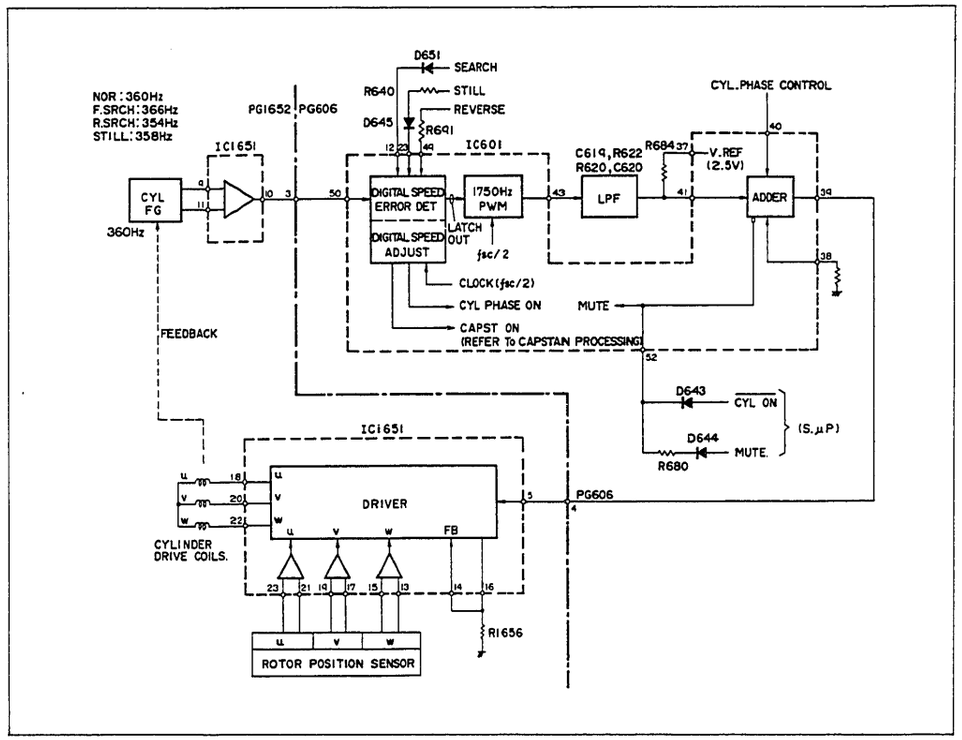


Fig. 3-4 Simplified Cylinder Speed Control Circuit Diagram

The PWM signal is supplied from pin 43 to a lowpass filter which generates a DC speed error correction voltage which is input via pin 41. The DC speed error correction voltage is applied to an adder circuit together with the phase error correction voltage from pin 40. The combined speed and phase error correction voltages generate a cylinder drive voltage at pin 39 of IC601.

During the stop mode it is necessary to stop the cylinder from rotating. To do this, a cylinder servo operation control command, "$\overline{\text{CYL ON}}$", is applied to pin 52 from the S-μP. When the voltage at pin 52 goes "Hi", the cylinder drive voltage at pin 39 becomes zero.

As with the cylinder speed, cylinder phase correction is performed in servo processing IC601. Fig. 3-6 is a simplified diagram of the cylinder phase control circuit. The cylinder tach signal is applied to the shaper at pins 4 and 5 of IC601. This shaper peak-detects the cylinder tach signal to form a pulse with a steep ramp. This output is applied to the tach selector. The tach selector selects the positive pulses of the cylinder tach signal in a VTR with 2 (or 3) video heads and selects the negative pulses in a VTR with 4 (or 5) video heads in the SP mode. This selection is determined by the voltage applied to pin 6 of IC601. To select

positive pulses, pin 6 is set to "Hi" (5V), and to select negative pulses, pin 6 is set to "Lo" (GND). Since the VT-1100A/1105A have 2 video heads, pin 6 is held at "Hi" (5V). The output of the tach selector is applied to the CH1/CH2 tach separator. The CH1/CH2 tach separator provides two outputs, a 30Hz signal which is applied to the switch 30Hz generator and a divided FG (60Hz signal) which is applied to the tach shift MM.

The delay of the tach shift MM is determined by time constant (RT601, C617) at pin 45. The output of the tach shift MM is applied to both the switching 30Hz generator and the cylinder phase error detection circuit. This delayed tach signal operates as the comparison signal for the cylinder phase error detection circuit.

During recording, the reference signal is developed from the composite sync signal which is applied to pin 53 of IC601. This composite sync signal is applied to a sync separator which supplies a 60Hz output. The 60Hz from the sync separator is applied to the cylinder phase error detection circuit and to the record control track pulse (CTL) generator. The record CTL pulse generator is triggered by the 30Hz sync signal from the sync separator and produces a 30Hz record CTL pulse whose duty cycle is set to approx. 70%. The record CTL pulse is applied through pins 60 and 59 to the control head to drive it.

During playback, the reference signal for the cylinder phase error detection circuit is developed by the reference 30Hz generator. A 3.58MHz signal is supplied from the signal processing circuit to pin 32 of IC601. The reference 30Hz generator counts down the 3.58MHz signal and supplies a 30Hz reference signal through the record/playback switch to the cylinder phase error detection circuit. This 30Hz signal is compared to the comparison signal from the tach shift MM. With a rate of 447kHz, the cylinder phase error detection circuit generates the phase error correction data. The phase error correction data is applied to the cylinder phase PWM circuit operating at a rate of 1.75kHz and controls the duty cycle.

As described earlier, the phase PWM duty cycle is set to 50% by a control signal from the speed loop during starting up. The PWM signal is applied to a lowpass filter at pin 44. The lowpass filter generates a DC phase error correction voltage and applies it to a limiter circuit. The limiter is provided to prevent the cylinder phase processing circuit from attempting to correct speed errors. Then the DC phase error correction voltage is applied to pin 40. The phase error and speed error signals are then applied to an adder circuit which develops the cylinder drive signal at pin 39.

Since the unit features noise-locked search in both forward and reverse, the cylinder motor must be phase locked. Cylinder phase lock during search is performed by adjusting the reference 30Hz. During forward search, the reference 30Hz signal is adjusted to 29.49Hz, and in reverse search, to 30.51Hz.

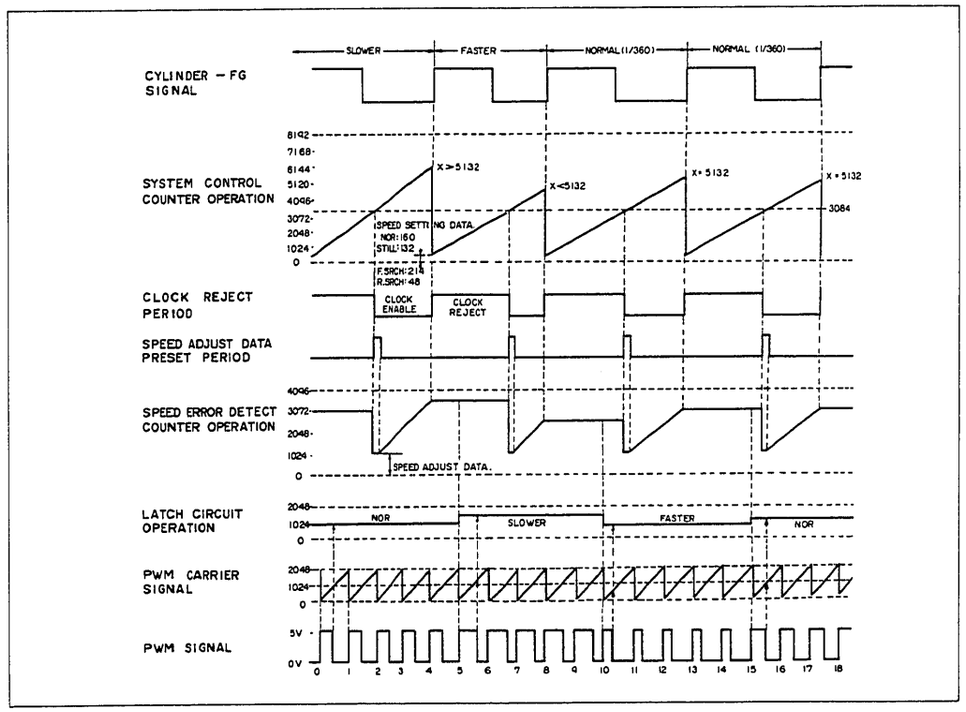


Fig. 3-5 Cylinder Speed Error Data Development

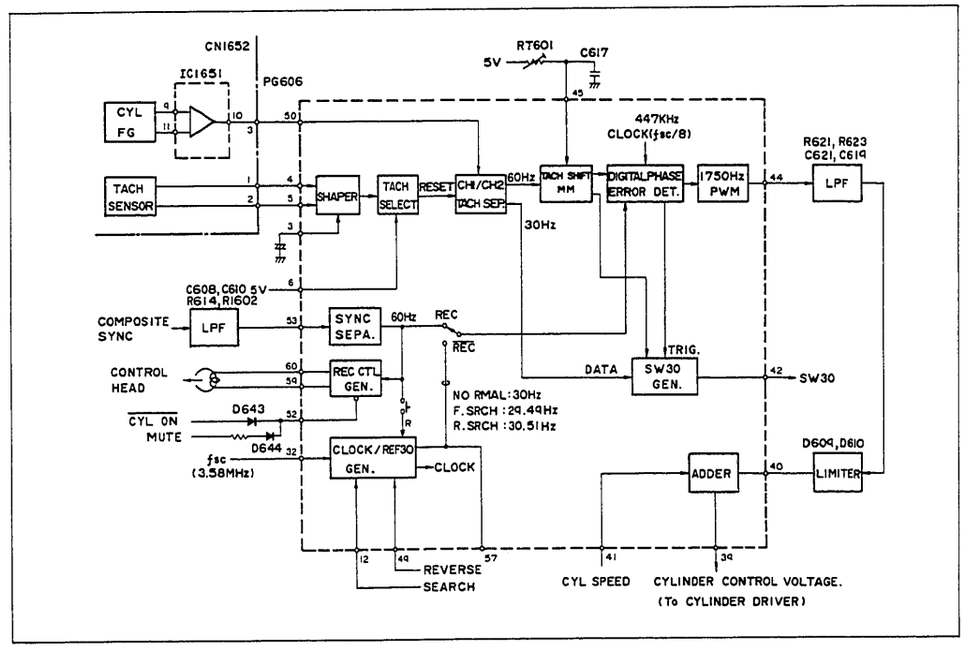


Fig. 3-6 Simplified Cylinder Phase Control Circuit Diagram

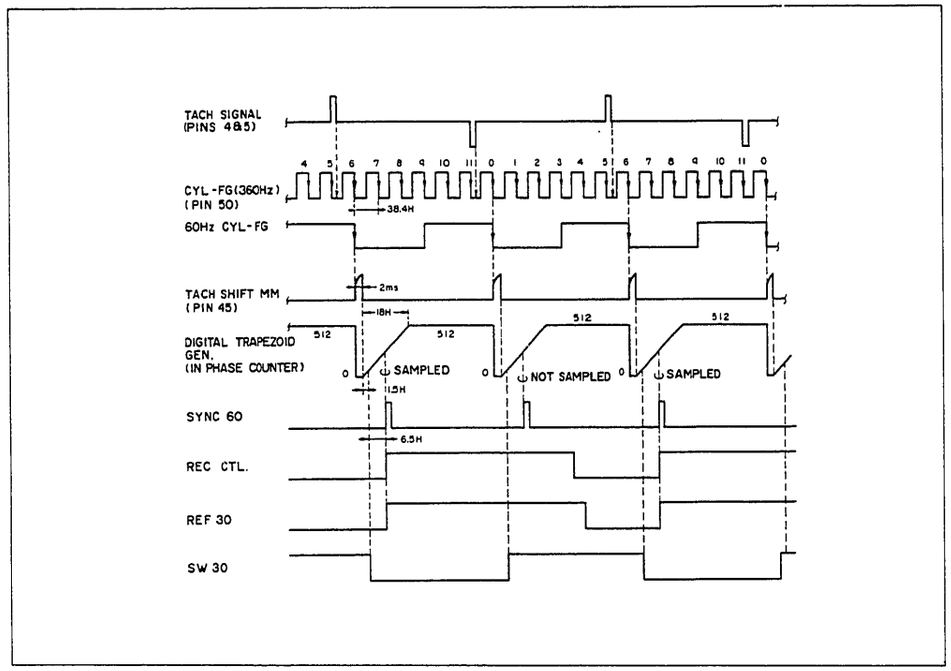


Fig. 3-7 Cylinder Phase Error Data Development

3-3-3 Capstan processing

The capstan speed processing circuit in IC601 is similar to the cylinder speed processing circuit. Fig. 3-8 is a simplified diagram of the capstan speed control circuit. The frequency of the capstan FG signal applied to pins 28 and 29 varies depending upon the speed of operation (SP, LP, EP). The capstan FG signal frequency is 720Hz in SP, 360Hz in LP, and 240 Hz in EP. The capstan FG signal is applied from pins 28 and 29 to the phase loop and a doubler (X2) circuit. During normal play and record operations, the X2 capstan FG signal is applied directly to the capstan speed error detection circuit for comparison.

During forward and reverse search, the capstan rotates at a faster rate and generates a capstan FG signal of 2160Hz. In order for the capstan speed processing circuit to operate correctly, the capstan FG signal must be divided down during search mode. This is performed by applying the SEARCH command, "Hi", to pin 12. A "Hi" at pin 12 routes the FG signal through the divide-by-3 circuit in the search mode. The reference signal for the capstan speed detection circuit is generated internally from a master clock which is divided down from 3.58MHz. This reference signal also varies depending on the mode of operation - 895kHz during SP or search, 447kHz in LP, and 298kHz in EP. Selection of the correct reference signal is controlled by the speed select circuit in IC601.

The digital capstan speed error signal is supplied from the error detection circuit to the capstan speed PWM operating at 3.5kHz and this controls the duty cycle.

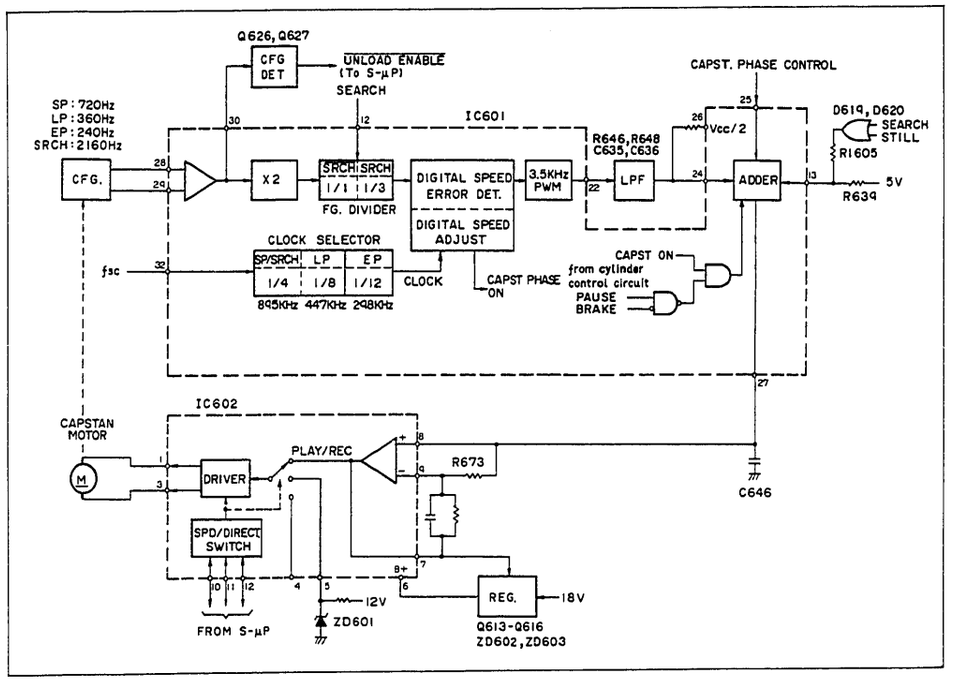


Fig. 3-8 Simplified Capstan Speed Control Circuit Diagram

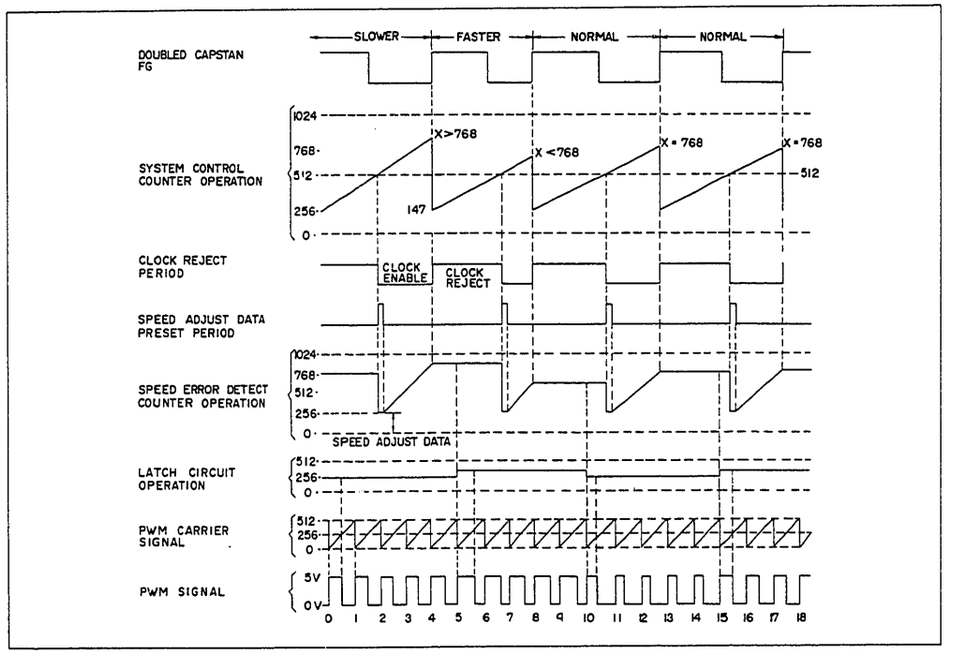


Fig. 3-9 Capstan Speed Error Data Development (in LP Mode)

The PWM signal is applied from pin 22 to a lowpass filter which generates a DC error signal. This speed error voltage is applied at pin 24 together with the phase error signal from pin 25 to an adder circuit.

The adder circuit is active when the capstan servo operation command, "CAPST ON", is applied from the cylinder processing circuit or when the brake pulse is generated in the interval brake pulse generator in the still mode. The "CAPST ON" command goes "Hi" when the cylinder motor reaches approx. 1314 rpm, at which point the capstan motor can turn on.

Capstan phase processing is similar to that of the cylinder. Fig. 3-10 is a simplified diagram of the capstan phase control circuit. During recording, the 30Hz feedback signal required by the capstan phase error detection circuit in IC601 is obtained from the capstan FG signal supplied at pins 28 and 29. Since the capstan FG signal frequency varies according to the speed of operation, it must be applied to the CFG 30Hz generator (FG divider). The CFG 30Hz generator divides the capstan FG signal by a different ratio for the different speeds of operation - by 24 in SP, by 12 in LP, and by 8 in EP. In the record mode, the capstan phase error detection circuit also receives reference 30Hz generated by applying 3.58MHz at pin 32 to the reference 30Hz generator. The capstan phase error detection circuit has a frequency of 447 kHz, which is generated by the master clock. By comparing the 30Hz that is generated by the CFG 30 generator and the reference 30Hz, the capstan phase error detection circuit supplies the digital data to the phase PWM. The digital data controls the duty cycle of the phase PWM which operates at 440 Hz, generating the phase error correction signal. The output of the phase PWM is supplied at pin 11 to a lowpass filter. Then the DC phase error correction voltage is applied to an adder circuit generating the capstan drive voltage at pin 25.

During playback, the capstan phase error detection circuit receives a feedback signal from the control track head at pins 59 and 60. The playback control (CTL) signal is applied to the amplifier and then through pins 62 and 63 to the CTL divider. During normal playback, the CTL signal is directly applied to the capstan phase error detection circuit. During search, it is necessary to divide the CTL pulse frequency depending upon the speed of operation. With this, the search signal is supplied at pin 12 to the CTL divider and the reference 30Hz generator. The 30Hz generated by the reference 30Hz generator is supplied to the tracking MM.

As was described previously, the VT-1100A/1105A feature noise-lock search. In order to maintain capstan phase correction during the search mode, the reference 30Hz must be adjusted. During reverse search, the reference 30Hz signal is 30.51Hz, and in forward search, it is 29.49Hz. The tracking MM provides a delayed 30Hz reference signal to the capstan phase error detection circuit. The delay of the tracking MM is controlled by the tracking presets and the tracking control, RV751, connected to pin 2 (on the front panel). The operation of the remaining capstan phase error detection circuit is identical to that in the record mode.

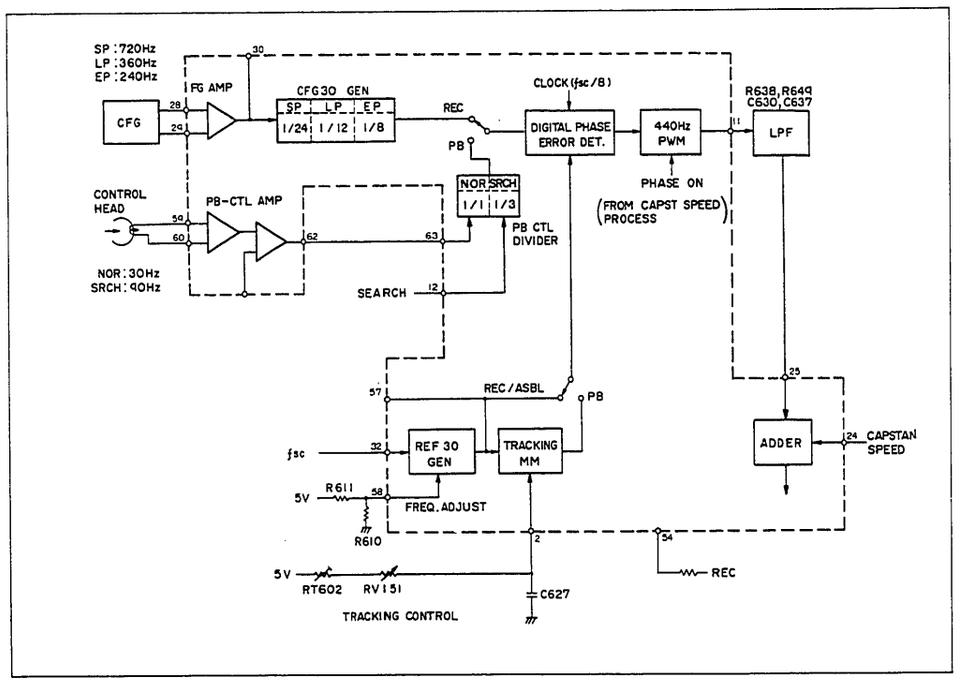


Fig. 3-10 Simplified Capstan Phase Control Circuit Diagram

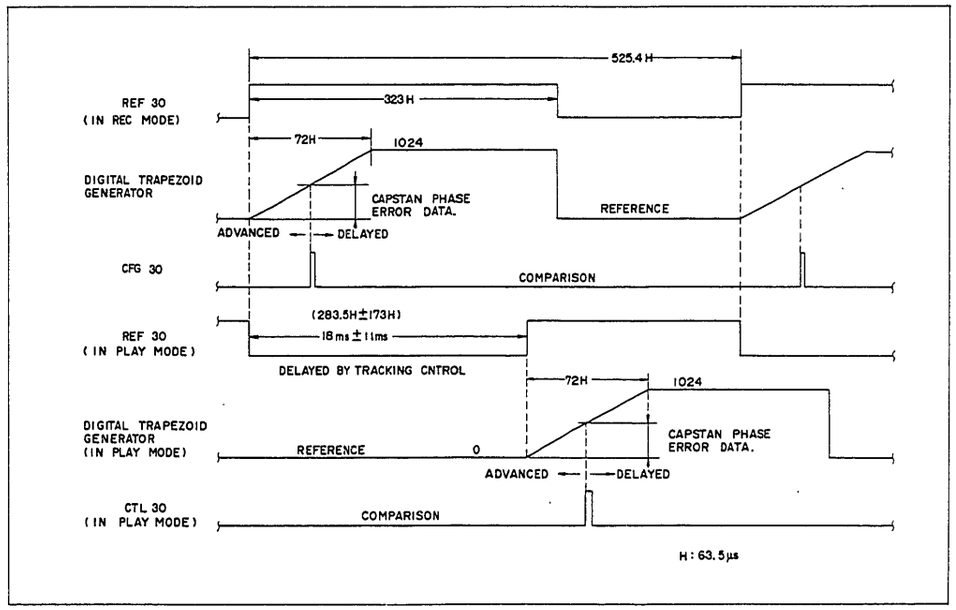


Fig. 3-11 Capstan Phase Error Data Development

3-3-4 Switch 30Hz generator

The tach detector and switch 30Hz generator provide the correct delayed switch 30Hz signal which is used for head switching and provided to the luminance/chroma and system control circuit. Fig. 3-12 is a simplified diagram of the switching 30Hz generator circuit and Fig. 3-13 is a head switching signal development. The switching 30Hz output at pin 42 of IC601 is developed by dividing down the 360Hz cylinder FG signal. The amount of delay introduced to the switching 30Hz output is determined by the delay through the tach shift MM and a fixed approx. 1.5H delay circuit. The tach shift MM is adjustable via the switching point adjustment, RT601, which is connected to pin 45 of IC601.

The cylinder tach and FG signals are applied to pins 4 and 50 respectively. The cylinder tach signal is supplied to the reset terminal of the FG divider circuit. The FG signal is applied to the clock input of the FG divider. By utilizing the tach pulse to reset the FG divider, it is possible to count down the cylinder FG signal of 360Hz to generate switching 30Hz. The FG divider develops two outputs: a 30Hz signal is developed by a divide-by-12 circuit, while 60Hz is developed by a divide-by-6 circuit. The 30Hz signal is applied to the D input of flip-flop 1. The 60Hz output of the divide-by-6 circuit is applied to the tach shift MM.

The delay of the tach shift MM is determined by the time constant at pin 45. A delayed 60Hz pulse from the tach shift MM is applied to the $\overline{CLOCK}$ input of flip-flop 1 and through another 1.5H delay to the $\overline{CLOCK}$ input of flip-flop 2. A 30Hz signal at the D terminal of flip-flop 1 is supplied to the $\overline{Q}$ output and applied to the D input of flip-flop 2. A 30 Hz signal from flip-flop 1 is delayed via the tach shift MM. The tach shift delayed 30 Hz at the D input of flip-flop 2 is then supplied to the Q output after a 1.5H delay. The Q output of flip-flop 2 is coupled to pin 42 and used as the switching 30Hz signal.

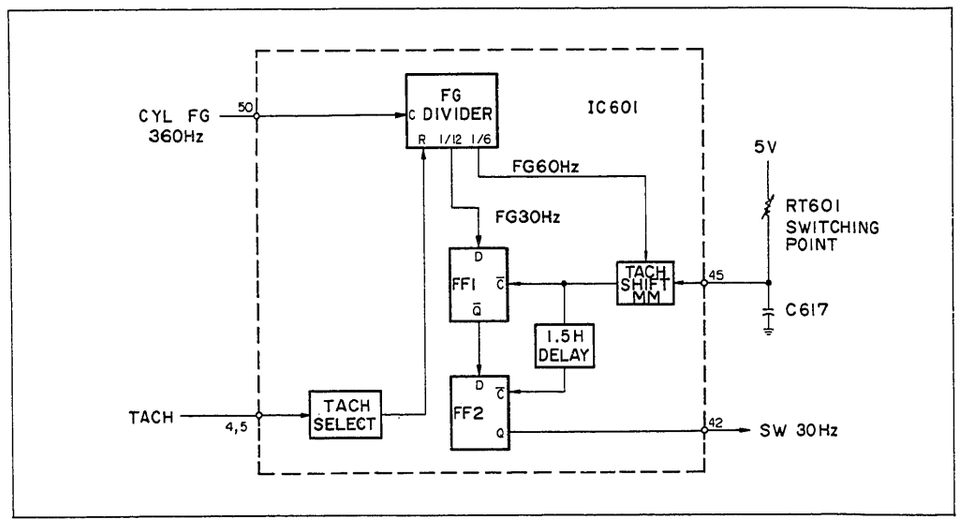


Fig. 3-12 Simplified Tach Detector/Switch 30Hz Generator Diagram

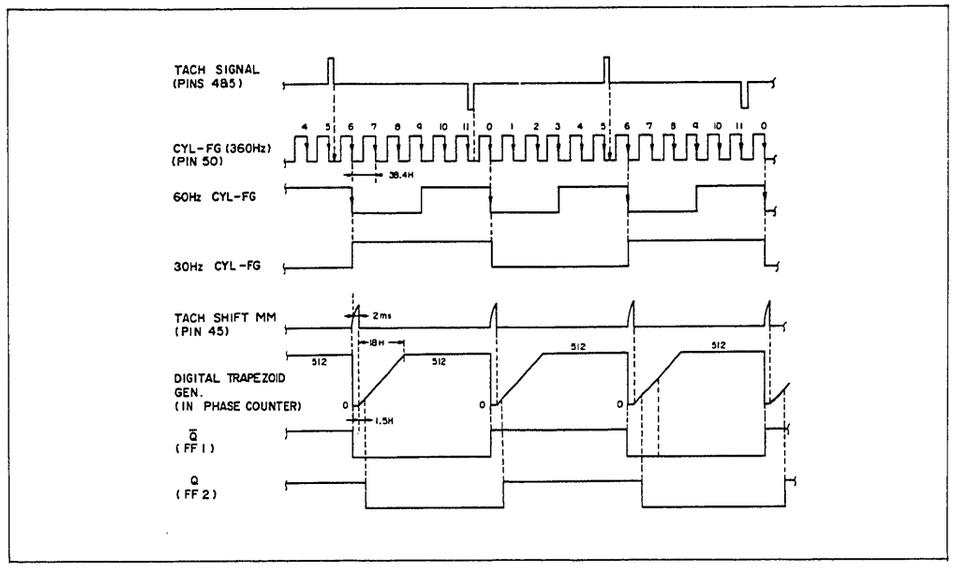


Fig. 3-13 Head Switching Signal Development

3-3-5 Tape speed selection/detection

The tape speed detection circuit determines the correct tape speed automatically during playback. The tape speed is selected manually during recording. Fig. 3-14 is a simplified diagram of the tape speed selection/detection circuit. The tape speed circuit in servo processing IC601, consists of three basic areas - playback speed detection, record speed selection and tape speed latch circuits. During playback, the speed detection portion of the IC receives two input signals -the capstan FG signal applied to pins 28 and 29 and the control track pulse applied to pins 59 and 60. The playback speed detection circuit divides the capstan FG frequency by the playback control track pulse frequency. The frequency of the capstan FG varies with the playback speed, (for example, it is 720Hz in SP, 360Hz in LP, and 240Hz in EP). The playback control track pulse frequency remains constant at 30 Hz. With the varying capstan FG frequency and constant playback control track pulse, the three tape speeds can be detected. This tape speed information is supplied to the playback section of a selector switch in IC601.

During recording, the internal selector switch is placed in the Record mode by supplying a "Mid" level signal to pin 54. Tape speed information is then supplied from the system control μP to the speed latch and generates the SP, LP or EP

signals at pins 9, 8 and 7 respectively. These signals are used in the luminance/chroma, audio and system control circuits.

During recording, the tape speed is determined by the record speed selection circuit, which receives a speed selection voltage corresponding to the tape speed information from the digital/analog (D/A) converter Q909. During SP, pin 10 is grounded meeting the criteria of the SP speed select voltage of less than or equal to 0.4 volts. Record speed selection determines the record speed is SP and provides an appropriate signal to the speed latch circuit.

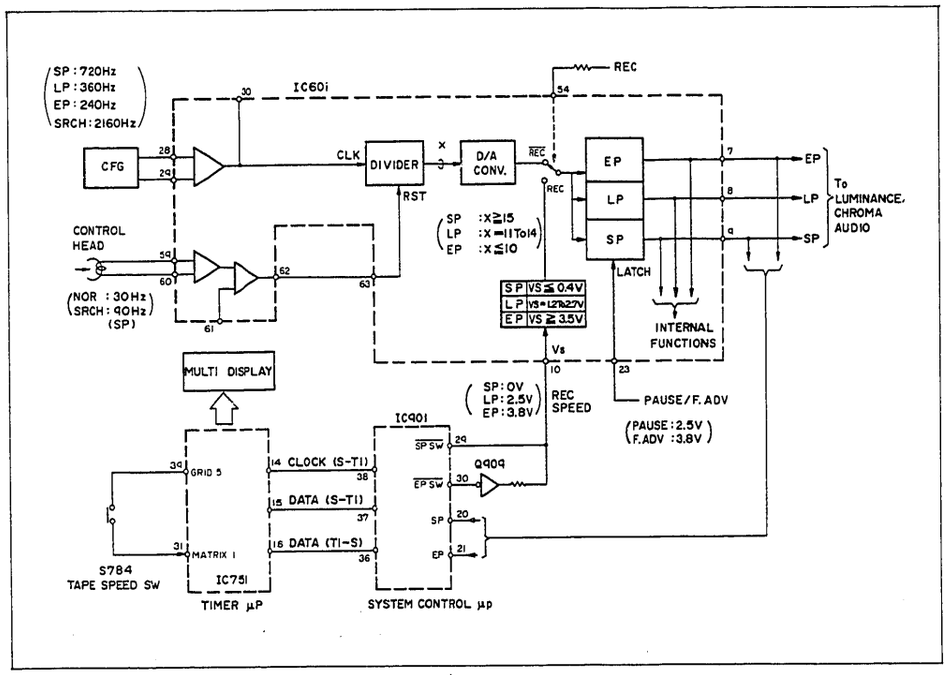


Fig. 3-14 Simplified Tape Speed Select Circuit Diagram

3-3-6 Start-up timing

Fig. 3-15 shows the timing chart for both playback and record operations. When either the PLAY or RECORD button is pressed, the loading motor immediately starts to load the tape and the video output is muted. At the same time, the cylinder speed loop is activated and the cylinder starts to rotate. Once the cylinder speed reaches approximately 1314 rpm, the capstan speed loop is turned on.

At approximately the same time that the capstan speed loop is turned on, the cylinder speed loop adjusts the free-running cylinder speed. The capstan is brought up to speed very quickly and performs the same free-running speed adjustment.

Once the cylinder speed loop has stabilized, the cylinder phase loop is turned on. (The cylinder phase loop is turned on approximately 2.5 seconds after the start of the loading sequence while the capstan phase loop is turned on after approximately 2.25 seconds. After three seconds the pressure roller is activated and starts moving the tape. After approximately 3.5 seconds, both the cylinder and capstan speed and phase loops are stabilized. After approximately 4.5 seconds, the video is unblanked).

In earlier servo systems, the free-running speed was obtained by the use of potentiometers and the speed varied depending upon such factors as humidity, temperature, age of the machine and mechanical friction, etc. To eliminate these variables, the servo system calculates the amount of drive required to obtain the free-running speed. Such as a cylinder speed of 1800 rpm. At the start of playback or record operation, a new free-running speed calculation is performed.

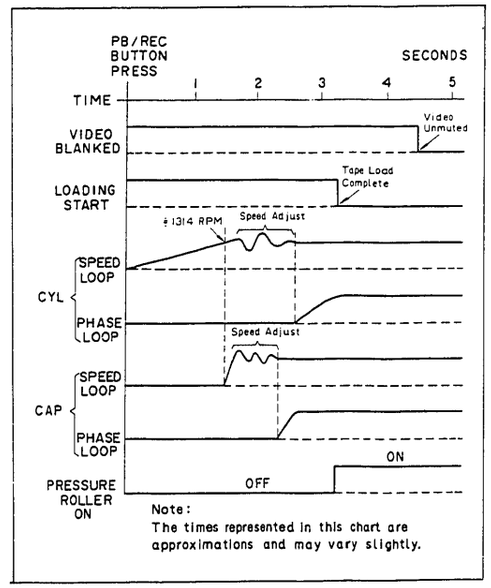


Fig. 3-15 Capstan and Cylinder Motor Startup Timing Chart

3-4 Assemble Control

3-4-1 General

When pause is instructed during recording and new audio/video signals are recorded on the previously recorded audio/video tracks, the assemble control minimizes noise when this section is played back.

Noise appears for the following reasons.

1. There is a non-recorded section between the end of the previously recorded section and the start of the newly recorded section.
2. The previously recorded video track and newly recorded track are not the same.
3. The cylinder speed and tape speed do not match at the start of newly recorded section.
4. Since the chroma level is high, the signal is not erased sufficiently.

To minimize noise, the following controls are performed.

1. Interrupts recording just after the pause mode is enetred and runs the tape in reverse for approx. 1.3 seconds (approx. 86 video tracks), then the compression between the capstan and pressure roller is released. After the pause mode is released, the pressure roller is compressed against the capstan and the tape runs. Recording is not done for approx. 0.9 seconds (approx. 54 video tracks: Assemble period) after the tape starts running and the control is performed to match the phases between the previouly recorded video track and the sync signal in the incoming video signal to be recorded.

These controls cause the following:

1. Since approx. 32 previously recorded video tracks are newly recorded (overlap recording), noise occurring due to cause 1 does not appear.
2. Since the phases of the previously recorded signal and incoming signal to be recorded are matched for approx. 0.9 seconds just after the pause mode is released, noise occurring due to causes 2 and 3 is reduced.

To reduce noise occurring due to cause 4, the recording current of the video signal to be recorded is increased for approx. 3 seconds (actually, 3 - 0.9 = 2.1 seconds) after the pause mode is released and the previously recorded chroma signal is erased sufficiently. Fig. 3-17 is a timing chart related to the amount of tape rewound and assemble control. The

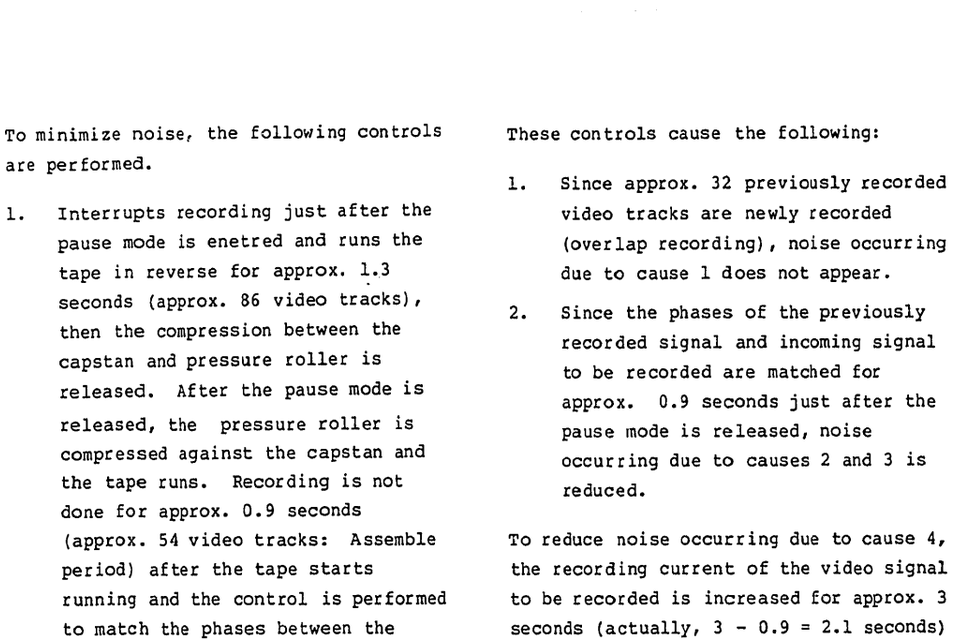


Fig. 3-17 Timing of Assemble Operation

system control μP generates the loading/capstan motor control, pause, mute and current up signals for the assemble control. The ASBL signal is supplied from the servo circuit.

- The loading motor switches the mechanism state in the order, REC/PB - REVERSE - REC PAUSE - REC/PB as shown in Fig. 3-17.
- The capstan motor runs the tape in reverse for approx. 1.3 seconds.
- The "PAUSE" signal sets the servo circuit to the pause mode.
- The "MUTE" signal inhibits the output of the REC 9V generator (Q416, Q407). It also inhibits recording of the control signal.
- The "CURRENT UP" signal lowers the feedback amount of recording video current and increases the recording current level of the video signal to be recorded.
- The "ASBL" signal has the same effects as the "MUTE" output.

3-4-2 Assemble operation in servo circuit

The servo circuit determines the assemble period and outputs the ASBL signal. In this period, the servo circuit plays back the previously recorded video tracks which are reversed just after the pause mode is entered, and synchronizes this with the phase (1/2 V. sync) of incoming video signal. Fig. 3-19 is a simplified diagram of the assemble control circuit and Fig. 3-20 is a timing chart of the assemble operation. The assemble period is determined by the ASBL MM in the main servo processing IC601. The ASBL MM is triggered when both voltages of "REC" applied to pin 54 and "PAUSE" to pin 23 reach 2.5V from 0V and generates a pulse with the period of approx. 0.7 seconds determined by the time constant (C654, R672) at pin 51. This pulse is used for the internal functioning of IC601 and is also derived from pin 55.

The control to synchronize the previously recorded video track with the phase of incoming video signal is performed in the main servo processing IC601. Fig. 3-18 shows an overview of cylinder and capstan phase control in the assemble mode. In the assemble mode, the video heads are phase-locked to the SYNC 30 signal in the incoming video signal via the TACH signal. The video track is phase locked to the REF 30 signal via the CTL 30 (control pulse) signal. Since the video

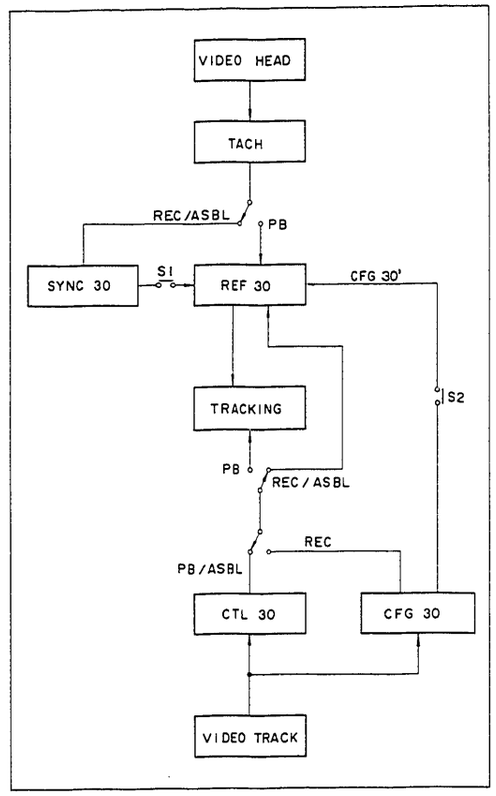


Fig. 3-18 Cylinder/Capstan Phase Control in Record Pause Mode

track must be phase locked to the video head, it is necessary to synchronize the phases of both reference signals (REF 30 and SYNC 30) for the video track and video head. To synchronize these phases, the phase of REF 30 signal is synchronized to the phase of SYNC signal and a preset value which sets the duty cycle of REF 30 signal to 93% ((525H-36H)/525H) is preset to the REF 30 counter generating the REF 30 signal. This causes the same effect as delaying the REF signal by an optimum amount with the tracking control during playback. When the assemble mode is released, the comparison signal of the capstan phase control loop is changed from CTL 30 to CFG 30, not changing the comparison signal of the cylinder phase control loop (Fig. 19). The preset command by the SYNC signal to the REF 30 counter via S1 is stopped. The phase of the CFG 30 signal is not synchronized with that of the CTL 30 signal, however, since the CTL 30 signal is phase-locked to the REF 30 signal in the assemble mode, the constant phase relationship is maintained between both signals. To minimize phase error when switching the comparison signal, one cycle of the CFG 30' signal the phase of which advances from the CFG 30 signal by approx. 36H is supplied to the REF 30 counter to reset it just after the assemble mode is released. The REF 30 counter generates a digital trapezoid wave for capstan phase control just after being reset, and when approx. 36H is reached, the data near the center slope of the digital trapezoid wave is sampled by the CFG 30 signal. Since the sampling data before and after the assemble mode is released are approximately aligned, a large phase error does not occur.

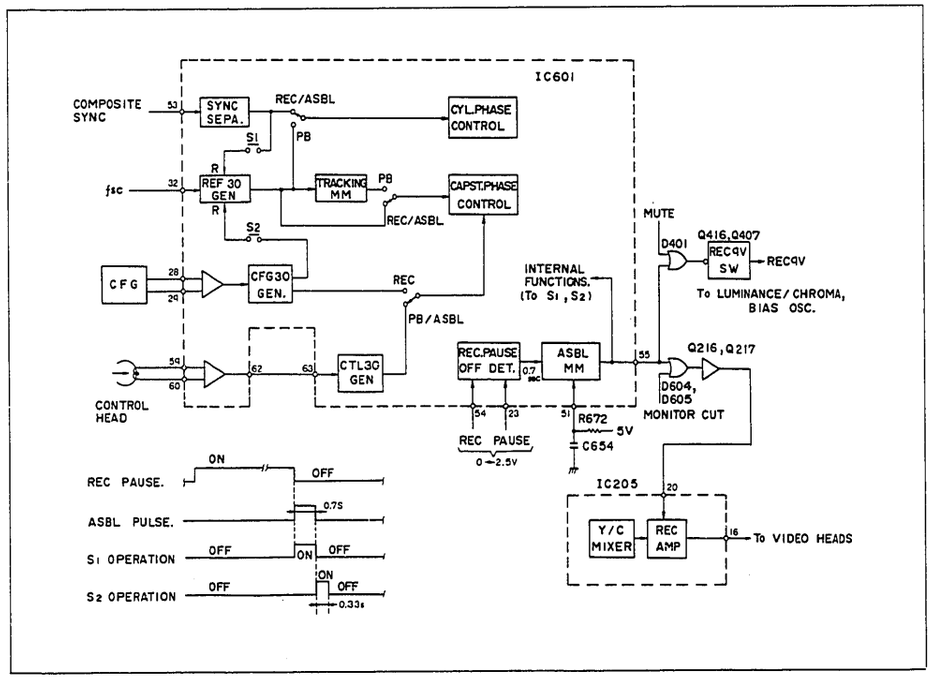


Fig. 3-19 Simplified Assemble Control Circuit Diagram

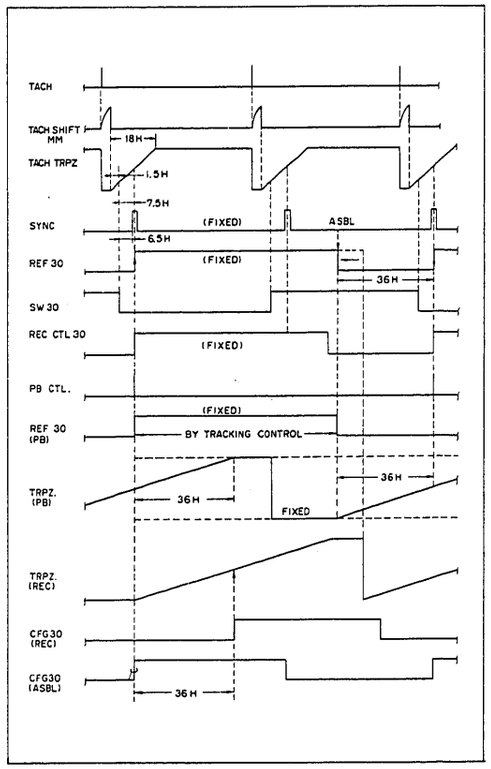


Fig. 3-20 Timing of Servo Circuit During Assemble Mode

3-5 Still/(Frame Advance/Slow) Operations (for VT-1310A/1305A)

3-5-1 General

The VT-1310A/1305A have field still play, frame advance and slow motion play functions. When the PAUSE button is pressed during play, the VTR enters the field still mode. The unit stops tape at one CH-2 video track aligning it with the scanning period of the video heads and plays it back. When the F. ADV button is pressed in the still mode, the VTR enters the frame advance mode and pulse-drives the motor to advance the frames while this button is held down. When the button is released, the VTR enters the still mode. When the SLOW button is pressed during play, the VTR enters slow motion mode and advances frames at approx. 1/10 the normal play speed automatically. When the PLAY button is pressed in the slow motion mode, this mode is released. The slow motion play is the same as when the F. ADV button is held down but different in setting and release methods. It is necessary to locate a CH-2 video track within the scanning period of the video heads and to minimize noise in the still, frame advance and slow motion modes. To do this control, the video track (tape) is stopped just before an optimum stop position, then the position in which the PB horizontal sync signal starts to be missing (this is assumed to be the tape stop position) and the optimum stop position are compared and the motor are pulse-driven until both positions are aligned. This optimum stop position is set to each edge of the head switching (SW30) signal.

3-5-2 Circuit composition and operations

Fig. 3-21 is a simplified diagram of the still/frame advance/slow control circuit. This circuit consists of the brake pulse generator, stop position error detector, fine advance pulse generator, driving timer, horizontal jitter canceler, capstan motor driver, still head selector, speed selector, speed up/down pulse generator and artificial sync generator. The following describes the main controls of these circuits.

Brake Pulse Generator:

Generates a brake pulse to stop the CH-2 video track (tape) at the optimum stop position instantaneously when pause is commanded. This circuit is triggered by the "PAUSE" mode setting signal which is synchronized with the phase of head switching signal by S-μP and generates a brake pulse whose phase (position) and width are set to optimum values and applies it to the speed/direction control inputs of the capstan motor driver. The capstan motor driver enters the reverse mode while this pulse is being applied. However, since the pulse width is short, the capstan motor stops just before it turns in reverse. This has the same effect as when braking is applied. The braking force is determined by the motor drive voltage of capstan servo in this braking period. After the braking period is passed, since the capstan motor driver enetrs the play mode, the brake pulse generator sets the capstan motor drive voltage to 0V and holds the capstan motor at the stop state.

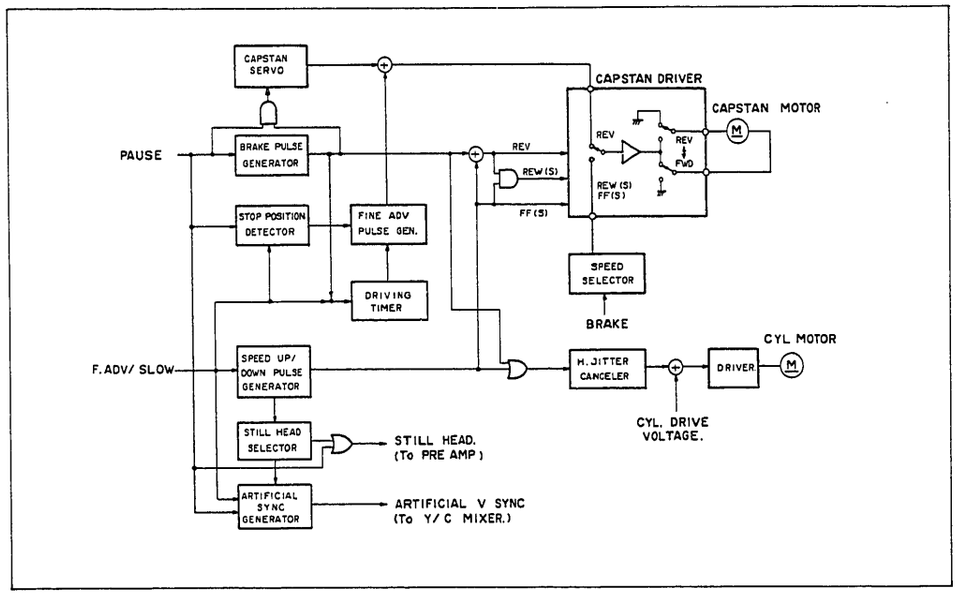


Fig. 3-21 Simplified Still/F.ADV/Slow Control Block Diagram

Stop Position Error Detector:

As soon as the tape is stopped by the brake pulse or speed down pulse in the still, frame advance and slow modes, this circuit detects the phase difference between the stopped video track (tape) position and optimum stop position. The video track stop position is determined by whether the PB horizontal sync signal starts to be missing or not. The optimum stop position is set to each edge of the head switching (SW30) signal. This detector output is applied to the fine advance pulse generator to trigger it.

Fine Advance Pulse Generator:

Generates a drive pulse to pulse-drive the capstan motor until the position error between the video track stop position and optimum stop position is eliminated. This output is applied to the REC/PB speed control input of the capstan motor driver. The capstan motor driver is set to the REC/PB mode by S-μP in the still mode, however, since the REC/PB speed control input is set to 0V, the tape is stopped. When the fine advance pulse is applied to the REC/PB speed control input, the capstan motor starts and advances the tape.

Driving Timer:

Limits the tape stop position fine advance period to a maximum of 4 seconds. Since a tape recorded by a VTR with 30 μm-width video heads in the SP mode has a non-recorded portion of approx. 30 μm width, the noise becomes wider than the stop position detection inhibit period of the stop position error detector and the stop position error output would always be output. This causes the tape fine advance operation not to be completed. To prevent this, the driving timer limits the fine advance period to a maximum of 4 seconds. This output is applied to the frame advance pulse generator to make it active.

Horizontal Jitter Canceler:

Cancels horizontal jitter occurring because the tape is tightly wound onto the upper cylinder when braking is applied to the capstan motor in the still, frame advance or slow mode. This circuit is triggered by both outputs of the brake pulse generator and speed up/down pulse generator and generates a cylinder speed correction pulse which has appropriate width and output. This pulse is added to the cylinder drive voltage to correct the cylinder speed.

Capstan Motor Driver:

Pulse-drives the capstan motor to stop or accelerate the tape. The pulse driving period is determined by both outputs of the brake pulse generator and speed up/down pulse generator. The capstan speed during the pulse-drive period is determined by the voltage selected by the capstan servo and speed selector. See the explanation given in the brake pulse generator and speed selector for details.

Still Head Selector:

Selects the head exclusively for still play which has the same azimuth as the CH-2 video head when

still-playing a CH-2 video track for field still play. This output is applied to the head switch control input of the video preamplifier circuit and artificial sync generator. The video preamplifier circuit selects the still video head and the artificial generator shifts the phase of artificial sync signal to correct it because the still video head is installed 2H before the CH-1 video head.

Speed Selector:

Selects the voltage for speed up or down in the frame advance and slow modes and the start speed setting voltage during fast forward according to the operation mode, and then applies it to the capstan motor. See the speed up/down pulse generator for deteils.

Speed Up/Down Pulse Generator:

Generates a speed up/down signal which is necessary to advance or stop the video track (tape) instantaneously in the frame advance and slow modes. The generator becomes active when receiving the "F.ADV" mode setting signal (Hi) applied from S-μP and generates the speed up or down signal every 450 ms. This output is applied to the horizontal jitter canceler and capstan motor driver. The horizontal jitter canceler is triggered by the speed down signal and generates a cylinder speed correction pulse. The speed up/down signal supplied to the capstan motor driver is converted to code "FF(S)" during the speed up period and to code "REW(S)" during the down period and is applied to the speed/direction control input. The rotation direction of the capstan motor is switched to forward with code "FF(S)" and to reverse with code "REW(S)", and the speed is determined by the capstan speed control voltage selected by the speed selector.

Artificial Sync Generator:

Artificially generates the vertical sync signal which is missing in the still play mode. This circuit becomes active when receiving the "STILL", "F.ADV" and "SEARCH" mode setting signals from S-μP, and the phase of artificial sync signal in each field is determined so the horizontal scanning frequency becomes 15.734kHz. This output is applied to the Y/C mixer in the luminance/chroma circuit.

4. AUDIO/VIDEO PROCESSING

4-1. General

Fig. 4-1 is a simplified diagram of the audio/video processing loop showing the route from the inputs to outputs and the relation between each μP. The audio/video processing circuit consists of the tuner/IF, input selector, audio/video processor, RF converter and output selector.

Tuner/IF:

Tunes the one of 107 programs receivable in the VHF and UHF bands using the voltage synthesis tuning system and supplies the tuned audio and video signals to the input selector. The controls necessary for tuning (4-band switching, tuning voltage control, defeat control, 80-channel list, auto frequency control) are performed by the tuning μP (TU-μP).

Input Selector:

Selects the audio and video signals applied to the audio/video processing circuit, commanded by the operator, from those supplied by the tuner/IF and line input jack, and supplies them to the audio/video processor. This switching is controlled by the timer μP (T-μP).

Audio/Video Processor:

Signal processing is different between the audio and video processor loops. The following tables show the main processing details of each processor loop.

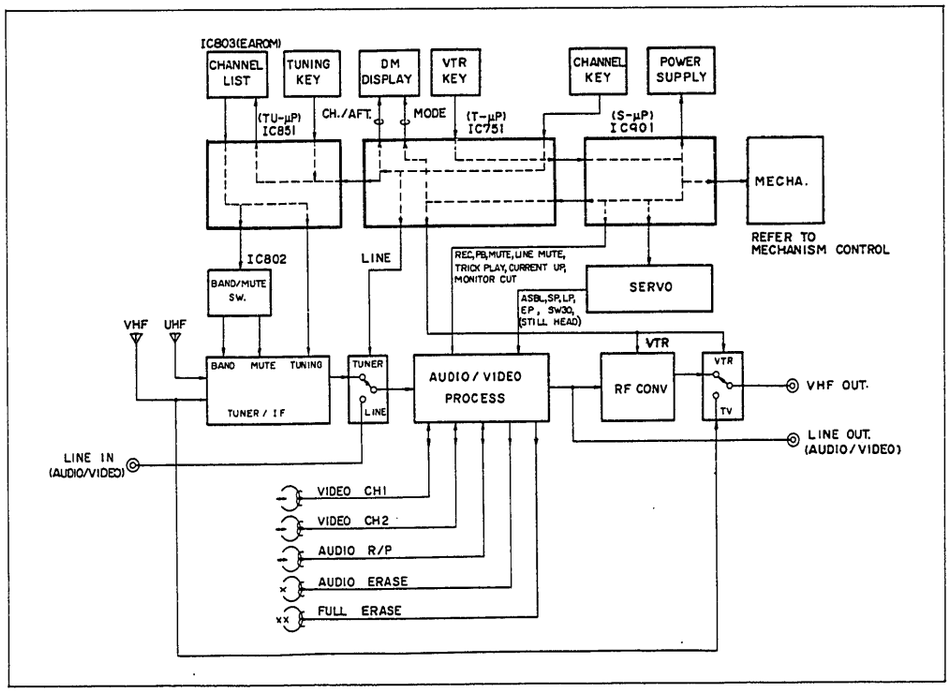


Fig. 4-1 AUDIO/VIDEO Control Block Diagram

The controls (mode change, muting, monitor cut, etc.) necessary for the above signal processing are performed by the system control μP (S-μP) and servo circuit.

RF Converter: Converts the monitor or playback audio and video signals to the RF signals in the exclusive VHF channel 3 or 4 band and supplies the RF-converted output to the output selector. The power supply for the RF converter is controlled by T-μP and becomes active when the VTR/TV switch is set to "VTR".

Output Selector: Selects the output from the VHF antenna or RF converter as a VHF output. This selection is controlled by T-μP in the same way as for the RF converter. When the VTR/TV switch is set to "VTR", the RF converter output is selected, and when the switch is set to "TV", the VHF antenna output is selected.

Audio Processor

Mode	Processing Details
REC	1. Adjusts the input signal to an optimum input level for the processing circuit. 2. Frequency-compensates the signal matching the tape speed to make the overall frequency characteristics flat in combination with the playback loop. 3. Adjusts the signal to an optimum recording current to be supplied to the audio record/playback head. 4. Amplifies the signal until it becomes the optimum monitor output and supplies it to the line output jack and RF converter.
PLAY	1. Amplifies the playback signal until it becomes an optimum level for the processing circuit. 2. Frequency-compensates the signal matching the tape speed to make the overall frequency character-istics flat. 3. Amplifies the signal until it becomes the optimum monitor output and supplies it to the line output and RF converter.

Video Processor

Mode	Signal	Processing Details
REC	LUMI-NANCE	The luminance signal is separated and the processing below is performed. 1. Adjusts the input signal to an optimum input level for the processing circuit. 2. Frequency-compensates the signal matching the tape speed in combination with the playback loop. 3. FM-modulates the signal to settle it in the specified frequency range. 4. Superimposes the down-converted chroma signal on the signal and adjusts it to an optimum recording current to supply it to the video heads. 5. Amplifies the signal until it becomes the optimum monitor output and supplies it to the line output and RF converter.
	CHROMA	The chrominance signal is separated and the processing below is performed. 1. Adjusts the input chroma signal to an optimum input level for the processing circuit. 2. Preemphasizes the chroma burst level by 6 dB in the SP and EP tape speeds. 3. Shifts the phase by 90° for every 1H and down-converts the chroma subcarrier frequency to 629kHz from 3.58MHz. 4. Adjusts the signal to an optimum recording current and superimposes the signal on the luminance signal. 5. Amplifies it until it becomes the optimum monitor output and supplies it to the line output and RF converter.
PLAY	LUMI-NANCE	1. Amplifies the playback signal to an optimum lever for the circuit. 2. Selects the preamplifier output and compensates the dropout to produce a continuous FM playback signal. 3. FM-demodulates the FM playback signal to return it to a video signal. 4. Frequency-compensates the signal matching the tape speed to make the overall frequency characteristics flat. 5. Amplifies the signal until it becomes the optimum monitor output to supply it to the line output and RF converter.
	CHROMA	The chrominance signal is separated from the FM playback signal and the processing below is performed. 1. Shifts the phase by 90° for every 1H and converts the chroma subcarrier frequency correctly to 3.58MHz from 629kHz to return it to the original frequency. 2. Amplifies the signal to an optimum level for the processing circuit. 3. Amplifies the chroma burst level by -6 dB to the original level in the SP and EP modes. 4. Eliminates the chroma crosstalk components.

4-2. Detailed Circuit Operations

4-2-1 Tuner/IF

The VT-1100A/1105A generate a digital signal representing the tuning voltage which is stored in an EAROM (Electrically Alterable Read Only Memory) instead of presetting the tuning voltage by a potentiometer. In the same way, the band and AFC information are converted to a digital code which is stored in the EAROM instetad of using mechanical switches.

Fig. 4-2 is a block diagram of the tuning system, TU-μP acts as the central controller in the voltage synthesis tuning system. The front panel tuning controls are input via the matrix switch to TU-μP together with the output of the infrared receiver. The EAROM acts as the storage medium for the digital code that represents the tuning voltage, the band, and AFC information. A 3-bit unidirectional bus from TU-μP is used to transmit address and command data to the EAROM. A single bidirectional bus is utilized to transfer the tuning data itself into and out of the EAROM. T-μP data is also input to TU-μP in order to accommodate timer recording functions where a preselected channel has been programmed into the VTR.

TU-μP outputs a muting signal coupled through switch circuit to the tuner/IF in order to blank video and audio during channel selection.

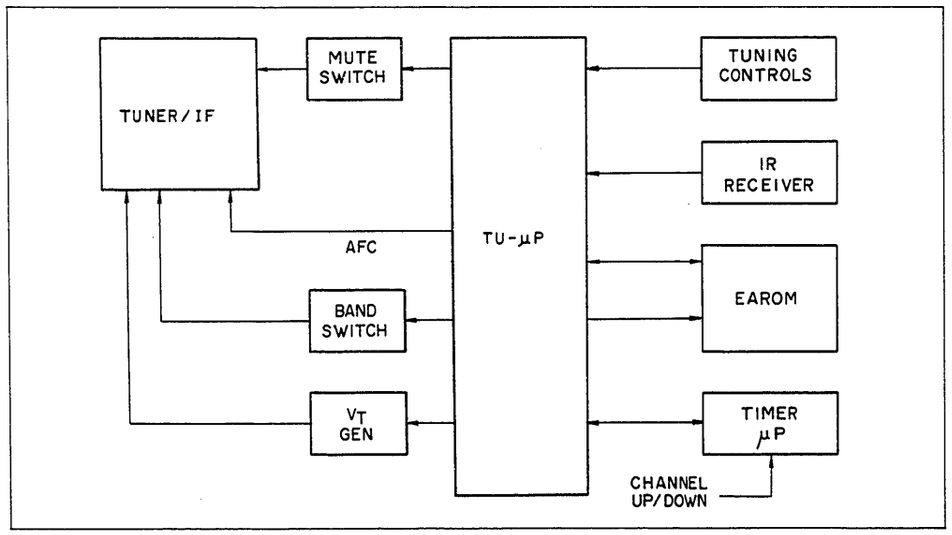


Fig. 4-2 Voltage Synthesis (VS) Tuning System Block Diagram

As shown in the simplified block diagram, TU-μP generates the band switching signal for the tuner and also generates the actual tuning voltage via the VT generator.

Tuning Voltage Generator

Fig. 4-3 is a simplified diagram of the tuning voltage generator circuit.

The tuning voltage output from pin 20 of TU-μP is a pulse width modulated (PWM) signal generated in TU-μP by utilizing the 13 bits of tuning data from the EAROM. The tuning data is then applied to a 7.8kHz PWM generator within the IC along with a 122Hz oscillator signal. The PWM output representing the DC voltage required by the tuner is applied to the base of Q802. The collector of Q802 is coupled directly to a lowpass filter allowing a DC voltage to be generated at pin 14 of PG802.

When TU-μP is tuning to higher frequencies, the "on" time of the pulse width modulated signal output from pin 20 becomes narrower, allowing more of the 33V DC supply to be supplied through the lowpass filter (LPF) to pin 14. This causes the DC voltage that is applied to the demodulator circuit board to increase. Conversely, when TU-μP is tuning to lower frequencies, the "on" time of the PWM signal output from pin 20 becomes wider, causing Q802 to be "on" longer and the voltage at pin 14 to decrease.

Fig. 4-4 shows the tuning voltage gradient when the tuning up button is pressed which is very shallow for approximately 1.5 seconds (fine tuning). After 1.5 seconds, the tuning voltage starts rising faster (coarse tuning). The band selected determines the per step voltage that is output from TU-μP.

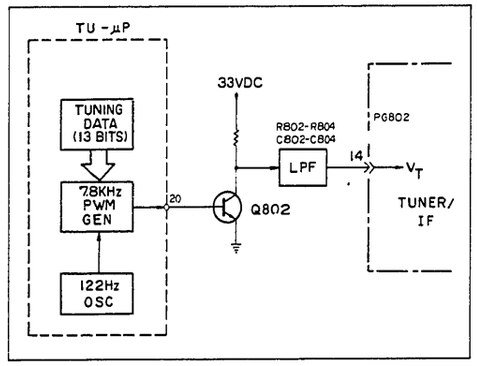


Fig. 4-3 Tuning Voltage (VT) Generator Circuit

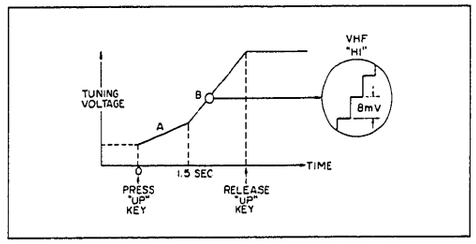


Fig. 4-4 Tuning Voltage Preamp

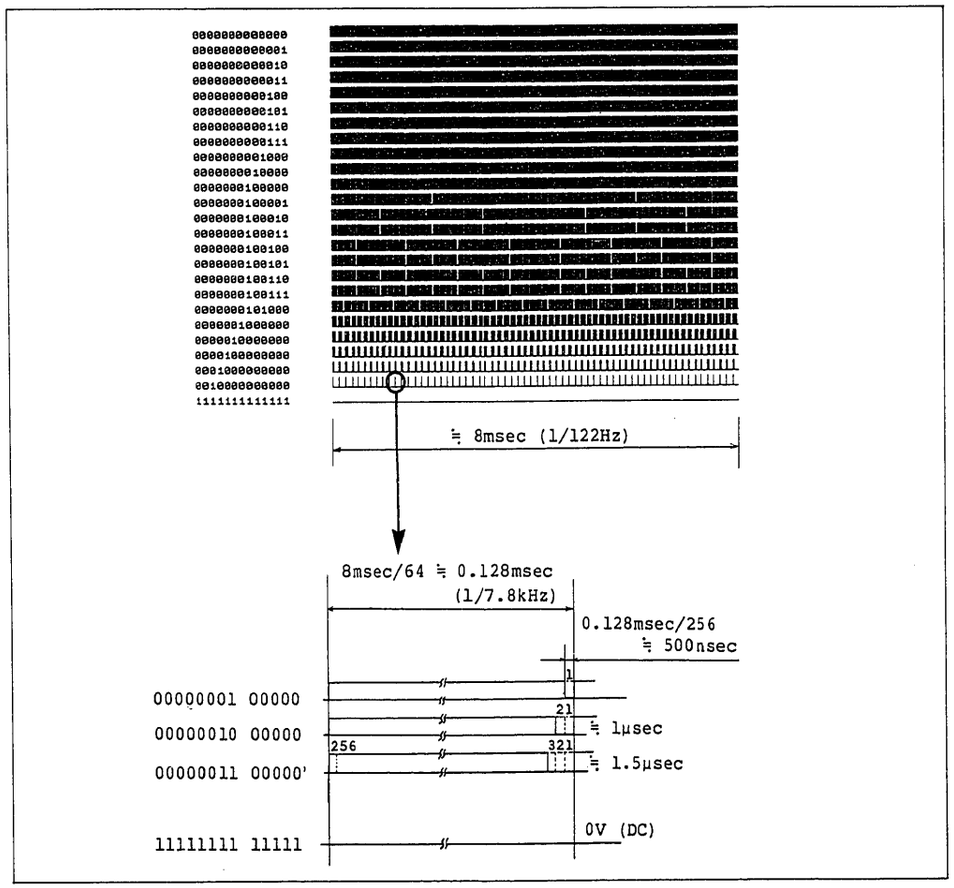
Table 4-1 shows the voltage synthesis tuning speed chart. When the tuner is searching the VHF "Lo" band, the PWM output of TU-μP changes approximately 15 times per second during the fine tuning operation. The PWM output changes 133 times per second during a coarse tune operation (approximately 12 mV per step). During VHF "Hi" and "Midband" operations, the tuner steps at approximately 10 times per second during fine tuning and 88 times per second during coarse tuning. This relates to approximately an 8mV change per step in the DC output of the lowpass filter.

Table 4-1 Voltage Synthesis Tuning Speed Chart

BAND	FING TUNING SPEED FIRST 1.5 SEC	COARSE TUNING SPEED	VOLTAGE PER STEP
VHF "Lo"	15/SEC*	133/SEC*	12mV
VHF "HI" and "MID"	10/SEC	88/SEC	8mV
SUPER	10/SEC	88/SEC	8mV
UHF	12/SEC	100/SEC	4mV

* STEPS PER SECOND

PWM GEN. OUTPUT (IC851 PIN 20)



Tuning Microprocessor-to-EAROM Communications

Fig. 4-5 shows the connections between TU-μP and EAROM. As mentioned before, TU-μP is responsible for the recovery of tuning information from the EAROM and also for writing information to the EAROM. To accomplish this, TU-μP outputs command data (3-bits) via pins 3, 2 and 1. These are referred to as command 1, 2 and 3 and are applied to pins 7, 8 and 9 of the EAROM, IC803. As shown in Table 4-2. Mode Command Chart, the commands output over the 3-bit (parallel) data bus consist of such commands as ERASE, ADDRESS SET, READ, DATA LOAD, WRITE, DATA STORE, etc. These commands instruct the EAROM as to whether information is being written to it (stored) or read from it (output) TU-μP over the data in/out (I/O) line. A clock signal is also output from pin 4 of TU-μP and input, to pin 6 of IC803 in order to synchronize communications between TU-μP and the EAROM. The data I/O line between pin 12 of IC803 and pin 13 of TU-μP first transmits the address of the data that is either being written to or read from the EAROM and then transmits the data itself.

A good example of normal operation is in the mode where a tuning voltage has already been input to the EAROM and the operator selects the channel. TU-μP first outputs the proper command on the command bus and then transfers the address of the data on the data I/O line. This is the actual address within the EAROM where the tuning data is located. TU-μP then transmits the necessary code over the command bus that instructs the EAROM to transmit the tuning data (13 bits) back to the TU-μP via the data I/O port. Fig. 4-6 and 4-7 show transfer timing to and from EAROM.

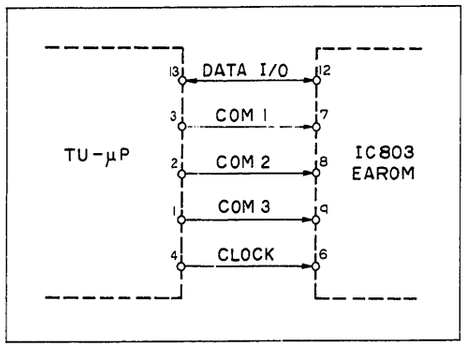


Fig. 4-5 Tuning μP EAROM Communication Bus

Table 4-2 Tuning μP to EAROM Mode Commands

COMMAND			FUNCTION
1	2	3	
H	H	H	STANDBY
H	H	L	NOT USED
H	L	H	ERASE
H	L	L	ADDRESS SET
L	H	H	READ
L	H	L	DATA LOAD
L	L	H	WRITE
L	L	L	DATA STORE

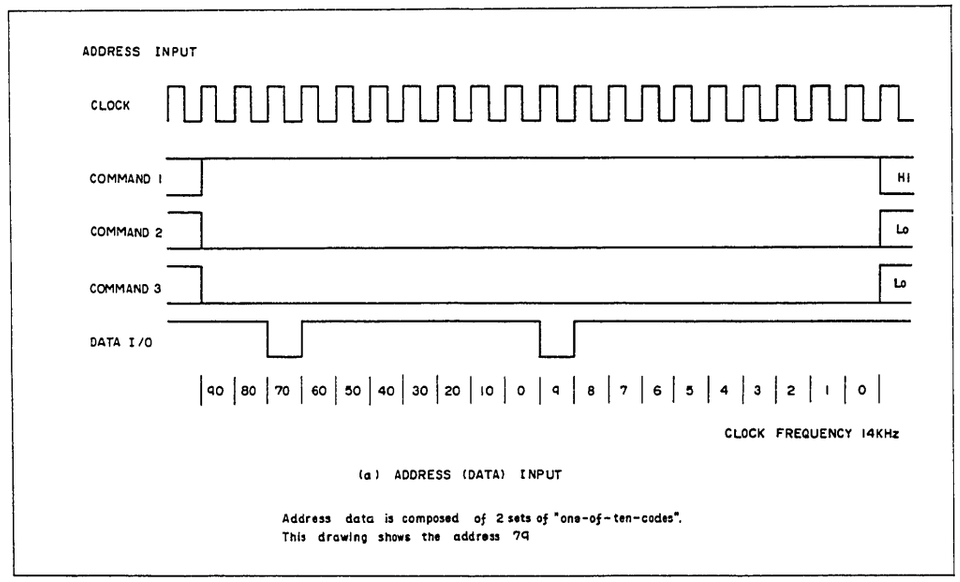

ADDRESS INPUT
CLOCK
COMMAND 1
COMMAND 2
COMMAND 3
DATA I/O
Hi
Lo
Lo
90 80 70 60 50 40 30 20 10 0 9 8 7 6 5 4 3 2 1 0
CLOCK FREQUENCY 14KHz
(a) ADDRESS (DATA) INPUT
Address data is composed of 2 sets of "one-of-ten-codes".
This drawing shows the address 79

Fig. 4-6 Transfer Timing to/from EAROM

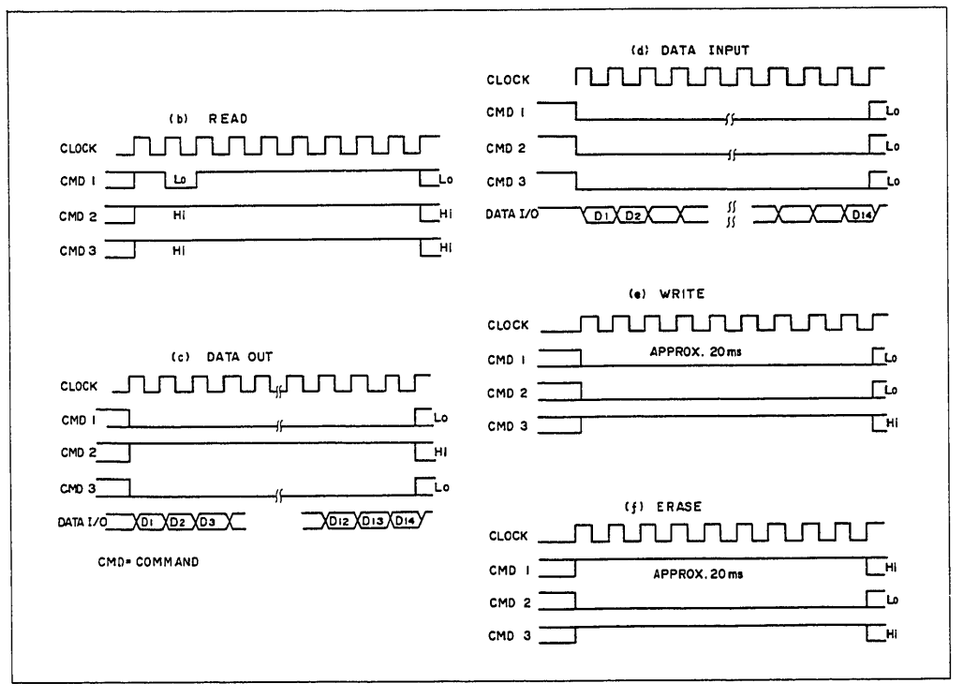


Fig. 4-7 Data Transfer Timing to/from EAROM

EAROM (Electrically Alterable Read Only Memory)

Fig. 4-8 shows a simplified block diagram of the EAROM. The tuning data information and the address of that information is applied to pin 12 of IC803 and fed into a buffer within the IC. The output of the buffer is applied to the appropriate register (data register or address register). The command information is input to the mode control circuit in IC803. The mode control circuit decodes the signal and applies the proper instructions to the memory section of the IC which has a READ, WRITE and ERASE configuration. As shown in the block diagram, the clock signal from TU-μP is also input to the mode control circuit in order to synchronize the read, write and erase functions. During the mode when the EAROM is being accessed for tuning data information, tuning data is output from the internal memory of the IC, first through the data register, then through the buffer, leaving the IC at pin 12 where it is then transmitted to the TU-μP via pin 13.

The total memory capacity of IC803 is 14 bits x 100 words, which allows a total of 80 channels to be stored in memory. The block diagram of the EAROM also shows two sections (or blocks) of address locations in the IC. These consist of address locations 0 through 79 and 80 through 99 - making up the 100 locations or words. The reason the memory is divided into two separate areas is described in the next section.

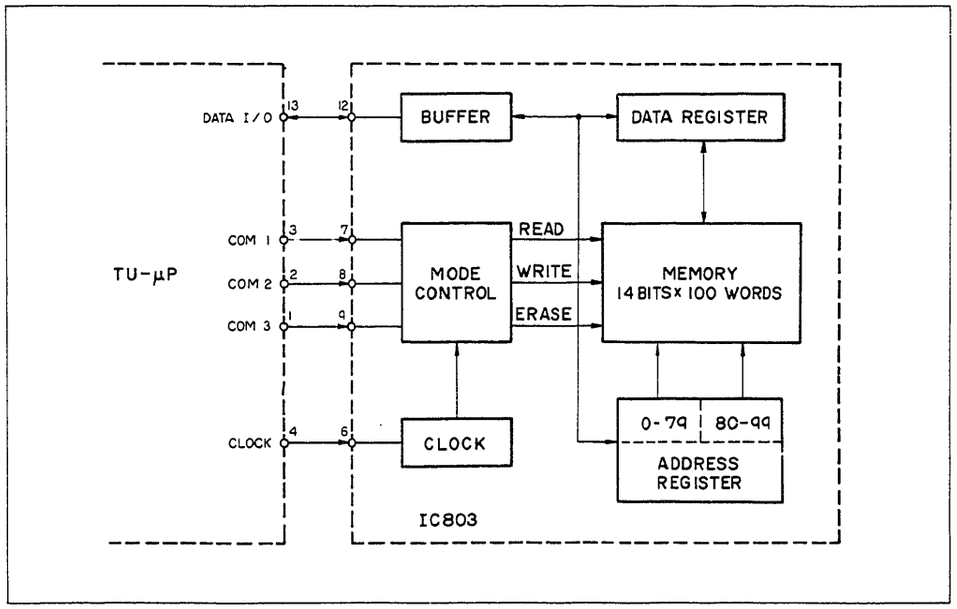


Fig. 4-8 Simplified EAROM Block Diagram

Fig. 4-9 is an EAROM memory map. Although there are 100 words in the EAROM, data only 80 channels can be stored, this is because band data and AFC data have also to be stored. At the top of the chart, for example, address 0 is designated as channel 1. The storage capacity of each address location is actually 14 bits, but only 13 bits of this is used for the tuning data itself and the last bit of the word is used to store the skip data. The skip data bit is required to allow the operator the option of programming out a channel he no longer wishes the tuner to stop at.

Once a channel (digital tuning data) has been stored in an address location, it cannot be erased except by writing over it with new channel information. For this reason, a skip command is needed in order to reprogram the tuner when the operator wishes to skip a channel that has been stored in the memory.

As the chart shows, there are 80 memory locations, 0 through 79, for tuning data. Memory locations 80 through 99 are allocated for the band data and AFC information. The exploded view of address location 80 shows the 14-bit word broken into four sections with 3 bits in each section (totaling 12 bits). The first 2 bits of locations 80 through 99 are not used. For example, when channel 41 is selected, the tuning data is first output from the EAROM. TU-μP automatically selects the proper 3 bits at address 80 that corresponds to channel 41. Again, this consists of 3 bits of information, 2 bits of which are the band where the channel is located and one whether the AFC is on or off.

Fig. 4-10(a) shows the data store sequence and Fig. 4-10(b) shows the data read sequence. A data store sequence occurs during initial setup of the VTR when the operator wishes to store an additional channel and place it in memory.

Starting at the "address set" block, the address or location of the tuning and skip data are placed in the EAROM. Moving next to the "erase" portion of the flowchart, the address location in the EAROM is automatically erased internally before storing the new tuning and skip data in this location. The data (tuning and skip) is next stored in the selected address location.

TU-μP now inputs the address where the band and AFC information is to be stored for the channel being stored in memory. Again, before the new information is stored in that particular memory location, any previous data is erased to ensure that the correct data is stored. Once the band and AFC data are stored in the EAROM, along with the tuning data, this information may now be recalled later.

The "data read" sequence is similar to the "data store" sequence. Instead of writing to the EAROM, TU-μP instructs the EAROM to read information out of the designated address into the TU-μP where it is converted to a DC tuning voltage. For example, the location or address of the tuning data of the desired channel is first placed in the EAROM. The EAROM reads the information from its memory, then loads this tuning data into its registers, and transfers the data to TU-μP. Next, TU-μP places the address of the band and AFC data into the EAROM. The EAROM reads the appropriate 3 bits of the band/AFC data into TU-μP where the band information is decoded. This allows TU-μp to switch the tuner to the proper band.

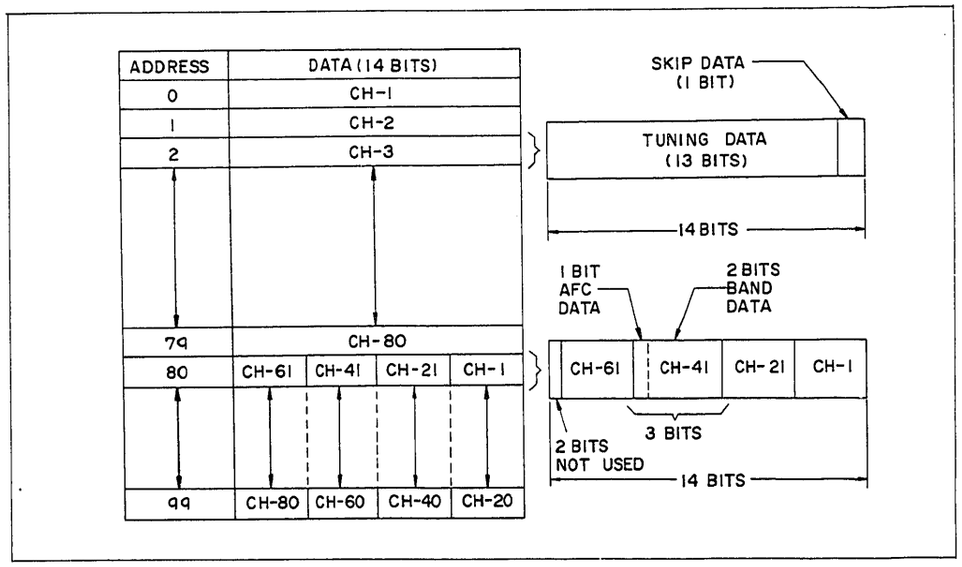


Fig. 4-9 EAROM Memory Map

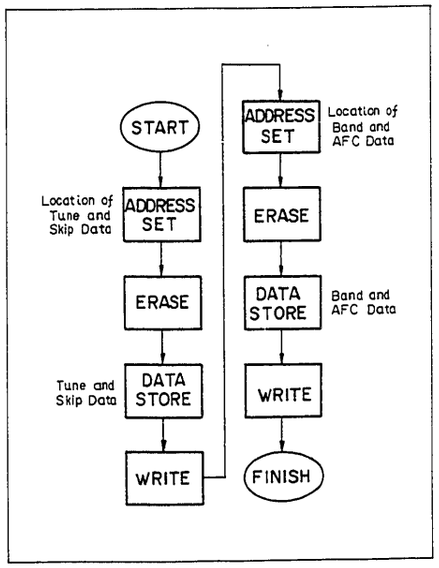


Fig. 4-10(a) Data Store Sequence

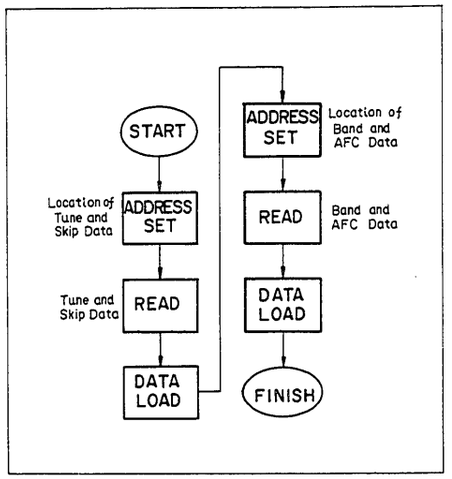


Fig. 4-10(b) Data Read Sequence

Band switching

Fig. 4-10(c) shows a simplified band switching diagram.
The circuit is very similar to that in other VTRs. TU-μP transmits a two-digit code to band decoder IC802 via pins 17 and 18. The two-bit output from TU-μP is decoded by IC802 and output as a 4-bit band switching singal at pins 17, 19, 18 and 20. They are applied via PG802 to the tuner/IF circuit board.

IC802 BAND DECODER	BAND			
	"Lo" VHF	"Hi" VHF	SUPER	UHF
B0 (Pin 5)	0	1	0	1
B1 (Pin 4)	0	0	1	1
D0 (Pin 17)	1	0	0	0
D1 (Pin 19)	0	0	1	0
D2 (PIN 18)	0	1	0	0
D3 (Pin 20)	0	0	0	1

Sandswitching Code Chart

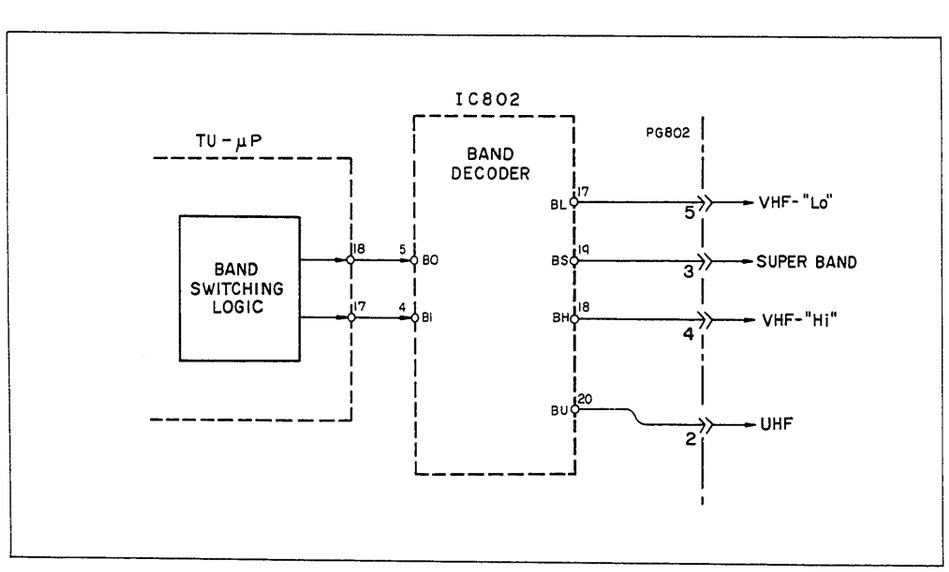


Fig. 4-10(c) Band Switching Circuit

4-2-2 Input Selector

Fig. 4-10(d) is a simplified diagram of the input selector circuit. TU-μP receives the LINE/TUNER information from T-μP via the communications lines, and every time TU-μP inputs the data, it determines LINE/TUNER signal output voltage at pin 9 to "Hi" (LINE mode) and "Lo" (TUNER mode) alternately. This output is applied to two input selectors. One is the video input selector IC501 at pin 3. IC501 inputs the video signal from the video input jack at pin 2 and the video signal from the tuner/IF at pin 7, and selects the video signal at pin 2 when pin 3 is "Hi" and the video signal at pin 7 when pin 3 is "Lo". The selected video signal is supplied to the luminance/chroma processing circuit. The other is the audio input selector/audio processor IC401 at pin 15. IC401 inputs the audio signal from the audio input jack at pin 14 and the audio signal from the tuner/IF at pin 16, and selects the audio signal at pin 14 when pin 15 is "Hi" and the audio signal at pin 16 when pin 15 is "Lo". The selected audio signal is supplied to the audio processor in IC401.

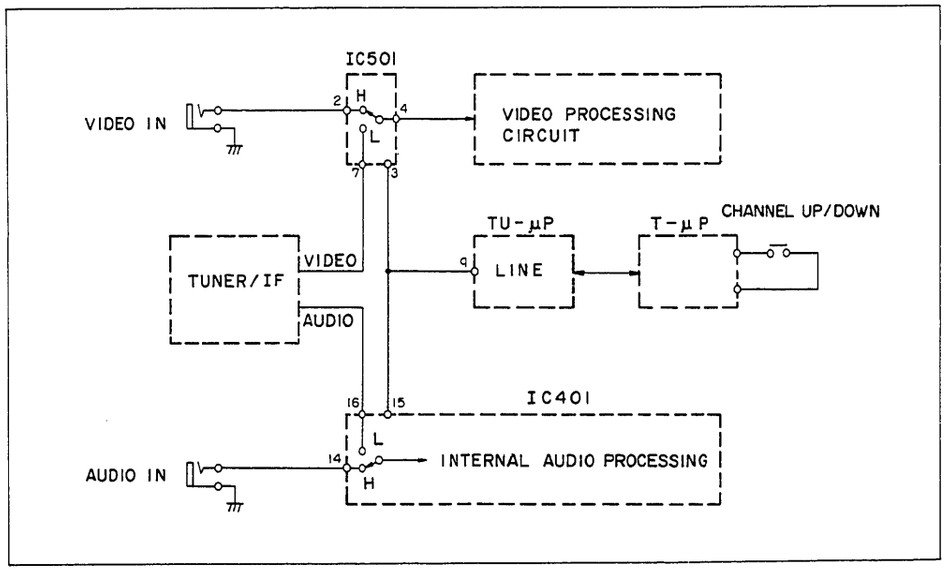


Fig. 4-10(d) Simplified Input Selector Circuit Diagram

4-2-3 Audio Processing Circuit

Fig. 4-10(e) is a block diagram of the audio circuit. One audio processing IC, IC401, controls the audio record processing, audio playback processing, bias ON/OFF operation and head operation.

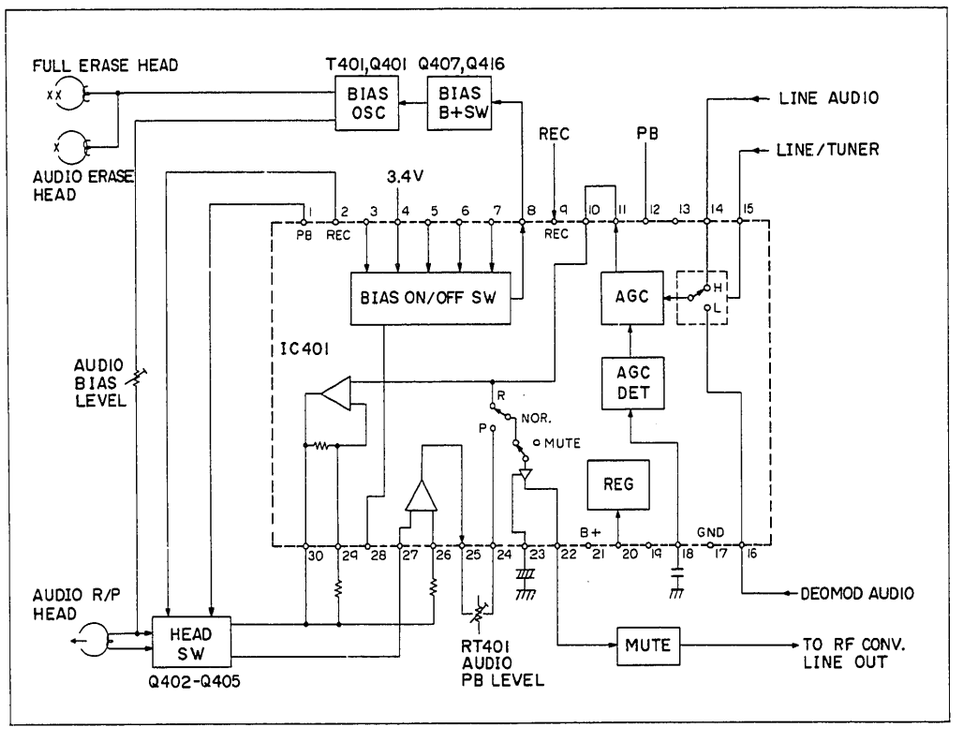


Fig. 4-10(e) Block Diagram of Audio Circuit

Audio record processing

Fig. 4-10(f) is a simplified diagram of the audio record processing circuit. When the VTR enters the record mode, the record mode setting input at pin 9 of IC401 goes "Hi". The "Hi" input at pin 9 changes over the REC/PB switches (S1/S2) in IC401 to "REC" and makes the bias oscillation controller active. The "Hi" input at pin 9 is also amplified and output at pin 2 to make the record head switch Q405 active. The audio signal supplied from the input selector descrived previously is amplified by the Line amplifier and leaves IC401 via pin 11. The signal reenters IC401 via pin 10 and is branched into two parts.
One is applied to the EE amplifier via S5 and is amplified. The output from the EE amplifier is applied to the AGC detector and EE/monitor output at pin 22. The audio signal at 22 is applied to the RF converter and audio output jack. The AGC detector rectifies the audio signal and filters it via capacitor C412 at pin 18, then applies it to the gain control input of the Line amplifier to determine the gain of the Line amplifier.
The other branched part is applied to the record amplifier. The record amplifier amplifies the audio signal matching the tape speed (SP, LP or EP) using the equalizer circuit at pin 29. The amplified audio signal is output at pin 30 and is applied to the bias signal from the bias oscillator circuit and is then supplied to the audio record/playback head to be recorded on the audio track. The power voltage and the voltage supply time for the bias oscillator is controlled by IC401. IC401 sets the internal bias ON/OFF switch active when pin 9 goes "Hi" and determines the power voltage (approx. 10.7V) for the bias oscillator at pin 8. This voltage is determined by the voltage applied to pin 4 and is set to approx. 3.4V. The output at pin 8 is applied to the base of the bias oscillator B+ switch Q407 to set the power voltage of the bias oscillator to approx. 10V. The base voltage of Q407 becomes zero when the "MUTE" signal supplied from S-μP or the "ASBL" signal from the servo circuit goes "Hi" to switch off the bias oscillator in the record pause and assemble modes. The "MUTE" or "ASBL" signal turns Q416 on and drops the base voltage of Q407 to zero. The bias oscillator output is derived via pins 5 and 6 of T401. The bias signal at pin 5 of T401 is supplied to the full erase head and audio erase head. Meantime, the bias signal at pin 6 of T401 is applied to the recording audio signal via RT402. RT402 adjusts the bias current flowing to the audio record/playback head to the optimum level.

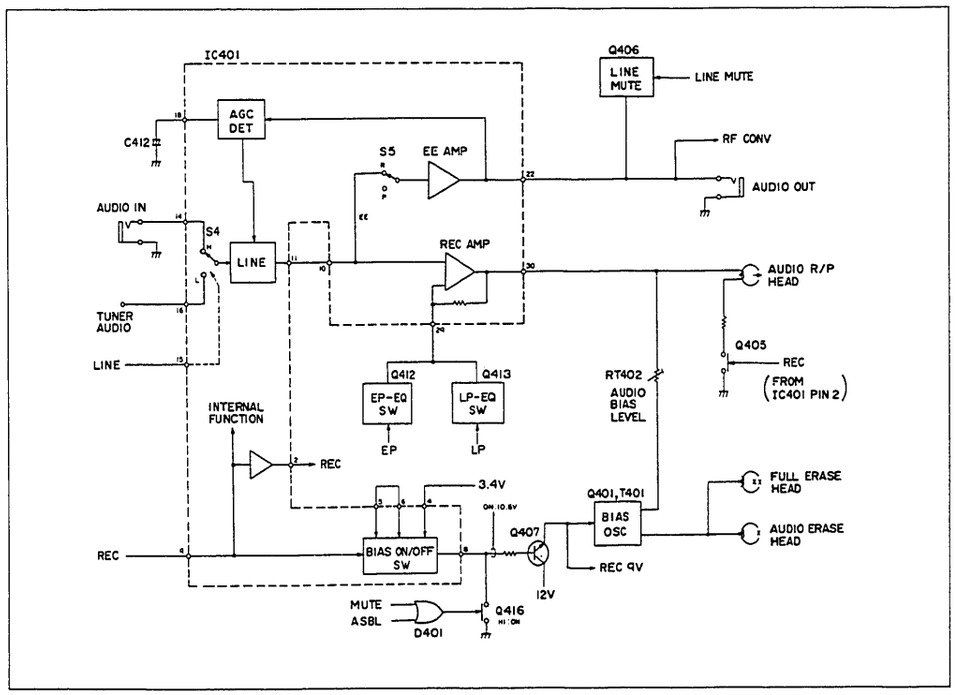


Fig. 4-10(f) Simplified Audio Record Processing Circuit Diagram

Audio playback processing

Fig. 4-10(g) is a simplified diagram of the audio playback processing circuit. When the VTR enters the playback mode, the playback mode setting input at pin 12 of IC401 goes "Hi". The "Hi" input at pin 12 changes over the REC/PB switch S1 in IC401 to "PB" and is also inverted by the internal inverter and is output at pin 1. The output ("Lo") at pin 1 is applied to inverter Q402 and is inverted to be "Hi" and is applied to the head switches (Q403, Q404). This causes Q403 and Q404 to be active and one terminal of the audio record/playback head is grounded. The audio signal picked up by the audio record/playback head is supplied to the preamplifier via the audio PB input at pin 27. The preamplifier amplifies the playback audio signal with very low level and also determines the amount of deemphasis matching the tape speed (SP or LP) using the equalizer circuit at pins 26 and 25. The amplified and emphasized audio signal is output at pin 25 and is supplied to the PB amplifier in IC401 via RT401, pin 24 and S1. RT401 adjusts the input level of the PB amplifier so it becomes the same level as in the record/E-E modes or the specified level. The PB amplifier amplifies the playback audio signal up to the level required for the RF converter and audio output jack. The amplified audio siganl is output at pin 22 and is supplied to the RF converter and audio output jack via line mute switch Q406. Q406 is switched on and off by the "LINE MUTE" signal supplied from S-μP and mutes the audio signal during trick play and loading modes.

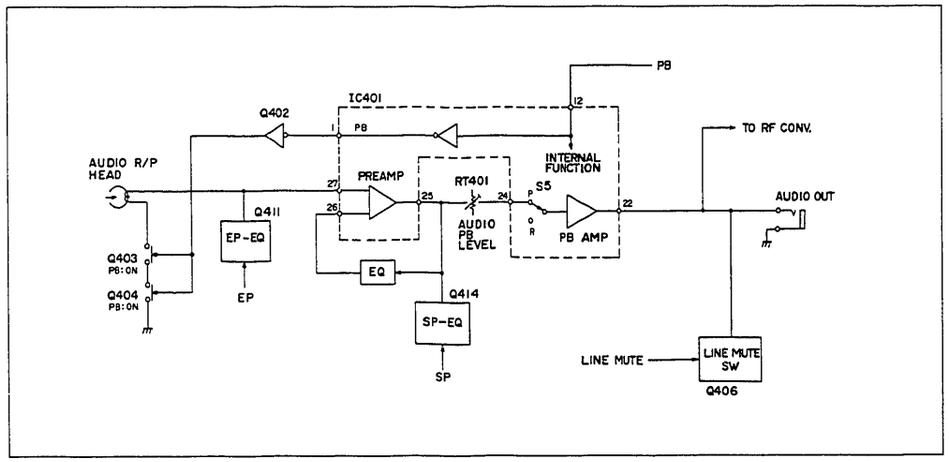


Fig. 4-10(g) Simplified Audio Playback Processing Circuit Diagram

4-2-4. VIDEO PROCESSING

(1) VHS HQ SYSTEM (Figs. 4-11, 4-12)

The VHS HQ (High Quality) system has been employed from this series of models VT-1100A, VT-1400A, etc. VHS HQ VTRs are compatible with conventional VHS VTRs. A VHS HQ VTR must satisfy two or more of the following conditions.

- o White clip level up 20% * (SP, LP, EP)
- o Detail enhancer (SP)
- o Luminance vertical processor
- o Chrominance vertical processor (This is not used in the VT-1100A/1105A.) EP only.

* This item must definitely be provided.

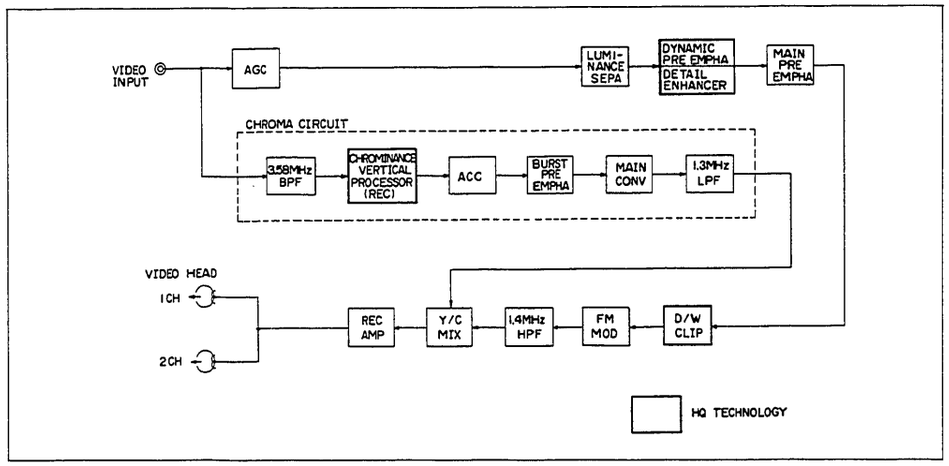


Fig. 4-11 VHS HQ System (Record)

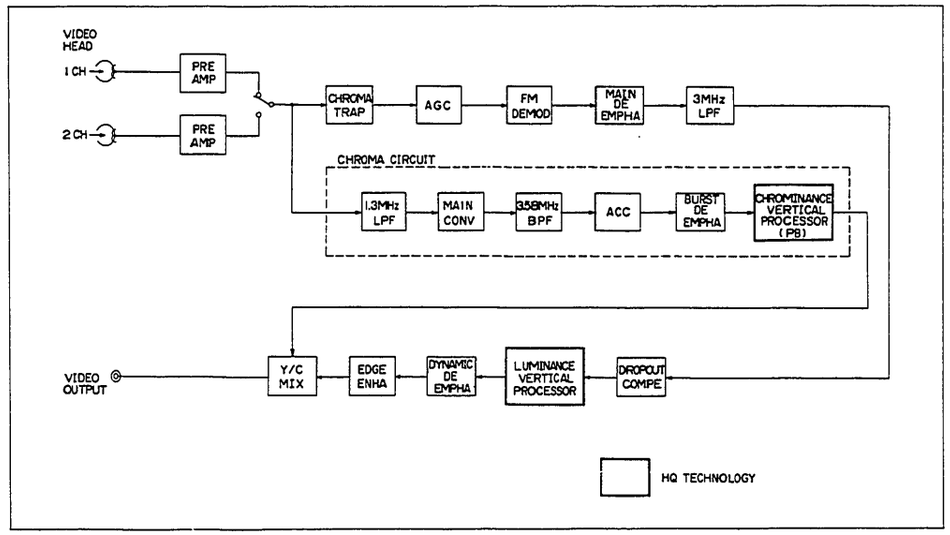


Fig. 4-12 VHS HQ System (Playback)

1) White clip level up 20% (Fig. 4-13)
Before the luminance signal is recorded, it is FM-modulated and mixed with the chroma signal and is then applied to the video heads. If noise occurring in the recording and playback loops enters the FM-modulated signal and the signal is FM-demodulated without any processing, the noise level becomes higher as the frequency is higher. Therefore, in a VHS VTR, the high-frequency components of the video signal are preemphasized by the preemphasis circuit before the signal is FM-modulated, and the high-frequency components are deemphasized by the deemphasis circuit after the signal is FM-demodulated.
When the high-frequency components are emphasized by the preemphasis circuit, overshoots are superimposed on the signal waveform as shown in Fig. 4-13 (c), and when the signal is FM-modulated, overmodulation occurs at the peak of the white peak level (shown by B in Fig. 4-13 (c)) and this may cause the picture quality to be degraded (black/white inversion). To prevent this, a white clip circuit was provided for the input of the FM modulator in previous VTRs. Since the characteristics of VTRs and video tape have improved recently, the clip level has been increased by 20% as shown in Fig. 4-13 (d) to improve the pulse response characteristics. As a result, the leading edges of the waveform (the edges in picture) where the black changes to white on the TV screen are played back more clearly.

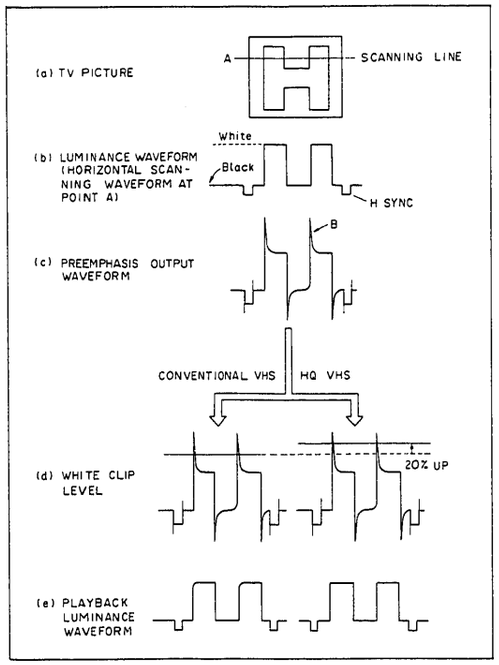


Fig. 4-13 White Clip Circuit

2) Detail Enhancer (Fig. 4-14)

When the video signal is recorded in the EP mode, dynamic preemphasis is applied to the video signal according to the signal input level to boost the medium frequencies (near 1 MHz) during recording in a conventional VTR. (Dynamic deemphasis is applied to the signal during playback.) This improves the S/N when the video signal level is low because the medium frequencies are boosted.
A detail enhancer changes the constants of the circuit using the dynamic emphasis circuit in the SP mode and enhances the high-frequencies of 3 - 4 MHz according to the input level of the video signal. Doing this during recording, the detail enhancer enhances the overall high-frequency response during playback as well as in recording. Therefore, when the signal is played back, an object with fine lines (such as a lawn, hair, etc.) can be seen more clearly. (This enhancer does not process the signal during playback.)

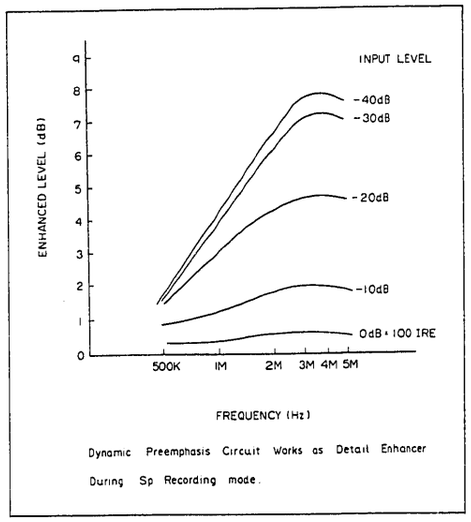


Fig. 4-14 SP Detail Enhancer

3) Luminance Vertical Processor (Fig. 4-15)

To improve S/N of the luminance signal, the line correlative noise canceler using a 1H glass delay line is employed in model VT-62A. This noise canceler averages the addition of the main playback signal and 1H delay playback signal and reduces the non-correlative noise such as white noise occurring during recording and playback to improve the S/N. To delay the FM signal by 1H by this method, another demodulator and deemphasis circuits were required as well as those for the main signal.

This new line correlative noise canceler (called as a vertical processor) uses a 1H delay circuit with a CCD and delays the signal by 1H in the base band (video signal) and comprises a feedback type noise canceler circuit. With this noise canceler, the S/N is improved, and a demodulator, deemphasis circuit and a control adjusting the level between the main and delay signals can be eliminated.
Fig. 4-15 shows the configuration of this vertical processor circuit. (This circuit also works as a dropout compensator and operates in all tape speed modes, SP, LP and EP.) The video signal demodulated by the FM demodulator enters IC205 via pin 25 and is output at pin 4 through SW1 and OP AMP 2. Part of this output signal is 1H-delayed by the CCD 1H DELAY circuit, IC204, and reenters IC205 via pin 3. The OP AMP 1 outputs the difference between the main signal and 1H-delayed signal. This difference signal A consists of the non-correlative

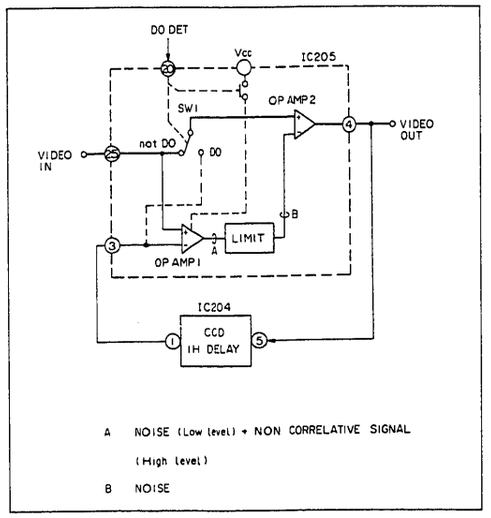


Fig. 4-15 Luminance Vertical Processor

noise component (white noise with low level) and the signal without vertical correlation in the video signal (generally, the signal with high level). Signal B is produced by applying signal A to the limiter which derives correlative noise with low level (white noise). The OP AMP 2 removes noise B from the video signal to improve the S/N.
As can be seen in Fig. 4-15, the vertical processor forms a feedback circuit. By circulating the signal twice and three times, the vertical processor overlaps the signals 2H before and 3H before to enhance the noise reduction effect. (The dropout compensation will be described separately.)

4) Chrominance Vertical Processor (Fig. 4-16, 4-17)

This circuit improves the chroma S/N in the EP (LP) mode and its basic principle is very similar to that of the luminance vertical processor. Fig. 4-16 is a basic principle diagram of this circuit during playback. The input signal (a) and 1H-delayed signal (b) are applied to the processor-2. Since the chroma subcarrier signal fsc has the phase shifted by 180° for every 1H, the processor-2 output in a picture with vertical correlation is only noise component (c) because two fsc signals cancel each other. Since the fsc component (with the level higher than the noise component generally) appears in the processor-2 output in a picture with no vertical correlation, the non-correlative component is eliminated by the limiter circuit in the next stage and the noise component (d) is

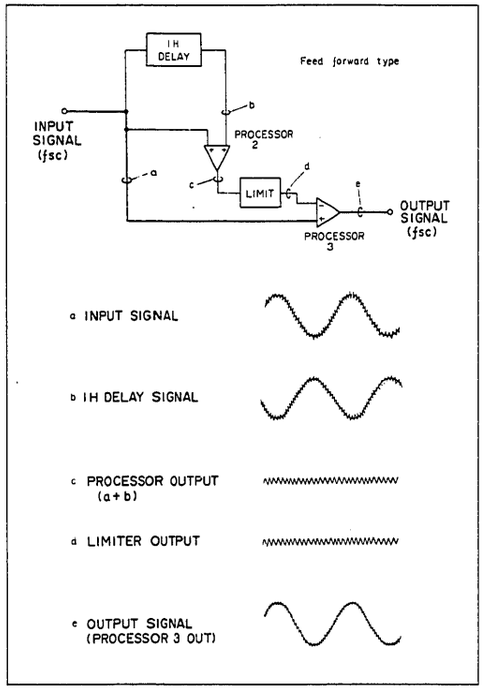


Fig. 4-16 EP Chrominance Vertical Processor (Ideal)

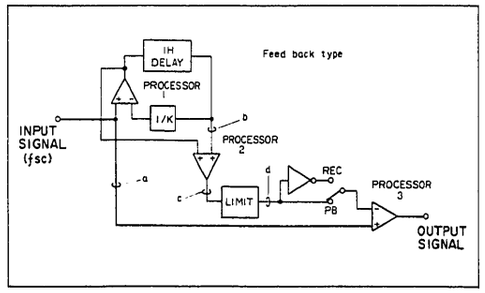


Fig. 4-17 EP Chrominance Vertical Processor (Actual)

derived, then this noise component (d) (limiter output) is subtracted from the original input signal (a) to improve the S/N.
In this principle diagram, no feedback circuit is present in the 1H delay circuit and a feed-forward circuit is formed so the signal used for noise canceling is only the signal 1H before. The circuit actually used is a feedback type as shown in Fig. 4-17, and feedback is applied with weighting of 1/K (approx. 0.7). The noise cancel effect is enhanced by making the weighting less in sequence also using the signals 2H and 3H before. When this system is employed, color smears occur slightly in the non-correlative section but this does not affect compatibility. To prevent this, the polarities of the limiter output shown in Fig. 4-17 are inverted and the signal in the non-correlative section is added in the processor-3 during recording to previously correct the distortion occurring during playback (a sort of preemphasis is applied).

(2) GENERAL

The video signal input to the video processing circuit is a composite video signal consisting of the luminance, chroma and sync components.

This circuit separates the composite video signal into the luminance signal (including the sync signal) and the chroma signal. Then the circuit FM-modulates the luminance signal to convert it to high-frequency components and converts the chroma signal to low-frequency components, then mixes the converted luminance and chroma signals to supply them to the video heads.

1) Overview of Luminance Record Processing Circuit (Fig. 4-19)

(a) AGC circuit
This circuit controls the input video signal so its output level is always constant regardless of level fluctuations in the input video signal supplied from the video input jack or RF converter circuit.

(b) Luminance separator circuit
This circuit extracts only the luminance signal components from the composite video signal.
Using a lowpass filter and comb filter, the circuit separates the luminance signal and chroma signal.

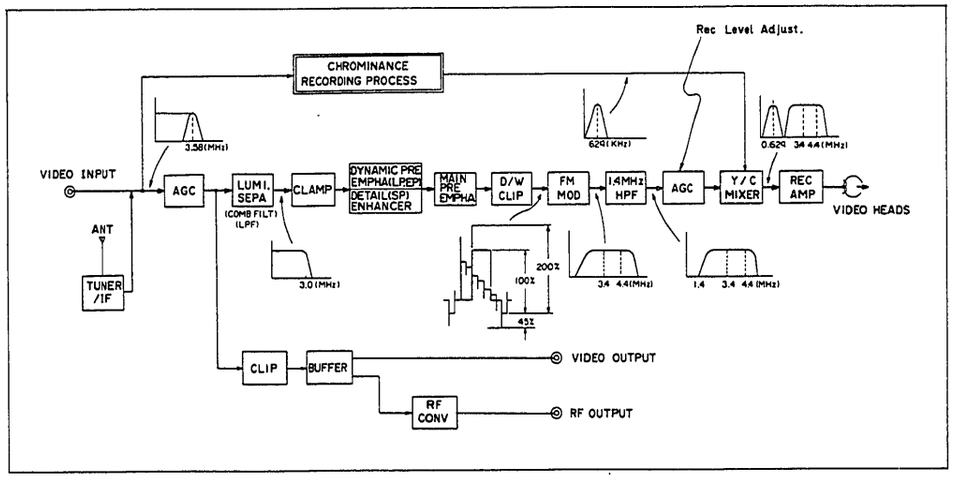


Fig. 4-19 Luminance Record Block Diagram

(c) Clamp circuit
This circuit fixes the DC voltage at the sync tip so it does not change due to the variation in the contents of the video signal. This is necessary for the dark/white clip circuit and FM modulator circuit in the later stage to operate normally.

(d) Dynamic preemphasis circuit
This varies the gain of frequencies centering near 1 MHz according to the input level of the video signal (picture components). When the input signal level is low (picture is dark), this circuit raises the video signal level centering near 1 MHz to improve the S/N. When the signal is passed through a circuit with the reverse characteristics (dynamic deemphasis circuit) during playback, the overall frequency characteristics become flat. This circuit works in the SP and EP tape speed modes.

(e) Detail enhancer circuit
This circuit boosts the high-frequencies of 3 - 4 MHz for recording when the input level of the video signal is low so that a lawn, hair, etc. with fine lines is seen clearly. This circuit works only in the SP mode.

(f) Main preemphasis circuit
As the frequencies of noise in the signal having passed through the FM modulator circuit are higher, its level becomes higher. This circuit emphasizes the high-frequency components of the signal previously during recording. During playback, the signal is passed through a circuit with the reverse characteristics (main deemphasis circuit) and the levels of high-frequency components are lowered, thus the S/N is improved.

(g) Dark/white clip circuit
When the video signal is preemphasized by the preemphasis circuit in the former stage, overshoots occur on the leading and trailing edges of the video signal. When it is fed to the next FM modulator as it is, overmodulation occurs; to prevent this, this circuit clips overshoots of the specified level or more.

(h) FM modulator circuit
The FM modulator circuit FM-modulates the video signal described above so that its sync tip is 3.4 MHz and the white peak is 4.4 MHz. However, this carrier frequency is shifted by approx. 1/2 fH (7.87 kHz) in CH-2 during the SP, LP and EP modes, to reduce beats interference due to crosstalk during play.

(i) 1.4 MHz HPF circuit
The HPF circuit attenuates the chrominance signal in the down-converted chroma signal band (629 kHz $\pm$ 500 kHz) to avoid color beats interference in the playback mode.

(j) AGC, Y/C mixer, recording amplifier circuits
The AGC circuit controls the luminance signal (FM modulated wave) output from the highpass filter so its recording current becomes constant, and the Y/C mixer mixes this AGC-controlled luminance signal with the chroma signal. The mixed signal is amplified by the recording amplifier and is then supplied to the video heads.

(k) E-E monitor circuit
After passing through the AGC circuit, the video signal is output via the clip circuit as an E-E monitor signal.

2) Overview of Luminance Playback Processing Circuit (Fig. 4-20)

Fig. 4-20 shows the main route and processing of the luminance signal in the playback mode.

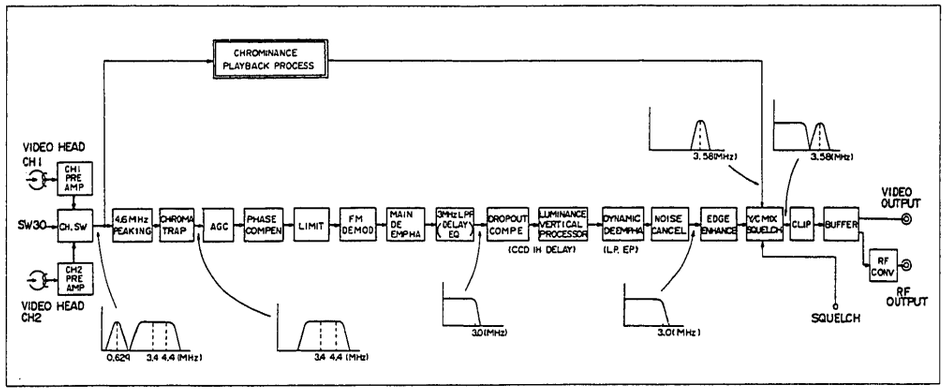


Fig. 4-20 Luminance Playback Block Diagram

(a) Preamplifier
CH1 and CH2 preamplifiers fully amplify the weak play signal picked up from the magnetic tape via the CH-1 and CH-2 video heads, and in addition, feed back the output of the preamplifier circuit to provide flat characteristics.
The same frequency compensation as in "60" Line models is performed by the equalizer circuit in the next stage.

(b) Channel Switch Circuit
The channel switch circuit switches the CH-1 or CH-2 signal using the SW30 signal to obtain a continuous signal.

(c) 4.6 MHz Peaking Circuit
As the frequency response of the preamplifiers in the previous stage is flat, the 4.6 MHz peaking circuit performs the same frequency compensation as in conventional models. That is, the 4.6 MHz peaking circuit compensates the head playback characteristics so that the total playback characteristics from the video heads until the 4.6 MHz peaking circuit are flat.

(d) Chroma Trap Circuit
This circuit removes the playback chroma signal (629 kHz) and supplies only the luminance

signal to the AGC circuit in the next stage.

(e) AGC Circuit
The AGC circuit operates so that the output level is always constant regardless of input level fluctuations, to prevent flickering due to the deviation and output level differences in the FM signal.

(f) Phase Compensation Circuit
The phase compensation circuit corrects the phase drift occurring in the 4.6 MHz peaking circuit described previously so that the video signal is not distorted during FM demodulation.

(g) Limiter Circuit
The limiter circuit removes amplitude variations in the FM signal. The limiter also limits the amplitude of the FM signal after boosting the FM high-frequency components to prevent black and white from being inverted. That is, the FM carrier output level becomes smaller than the low-frequency sideband level in the high modulation section of the played back FM signal causing distortion; when it is demodulated via the FM demodulator as it is, black/white inversion occurs. The limiter circuit prevents this.

(h) FM Demodulator Circuit
The video signal has been FM-modulated so that its sync tip is 3.4 MHz and its white peak is 4.4 MHz during recording, so the FM demodulator circuit demodulates it to the original video signal during play.

(i) Main Deemphasis Circuit
The main deemphasis circuit has reverse characteristics to the main preemphasis circuit used during recording; this circuit improves the S/N ratio while returning the high-frequency components emphasized by the preemphasis circuit during recording to its original value.

(j) 3 MHz LPF Circuit (Delay Equalizer)
The 3 MHz LPF circuit eliminates the FM carrier with its frequency 3.0 MHz or more remaining in the video signal demodulated in the previous stage. The delay equalizer circuit is also used for delay to match the luminance phase with the chroma signal, the same as in recording.

(k) Dropout Compensation Circuit
The dropout compensation circuit corrects dropout in the FM signal caused by either dust or dirt on the tape, poor or irregular tape coating and prevents picture noise from occurring.
This circuit utilizes the 1H delay circuit in the video signal band using a CCD to compensate for dropout.

(l) Luminance vertical processor
This is a noise canceler circuit which uses 1H correlation of the video signal.
This noise canceler uses a 1H delay circuit with a CCD (used in common with the circuit operated in the dropout compensation circuit described previously) and delays the signal by 1H in the base band (video signal) to comprise a feedback type noise canceler circuit.

(m) Dynamic Deemphasis Circuit
As described in the item "Luminance Recording Process", the dynamic preemphasis circuit varies the amount of emphasis according to the record signal level. The dynamic deemphasis circuit is provided with the characteristics in reverse to that of the dynamic preemphasis circuit; this varies the attenuation of the high-frequency component according to the playback signal level and returns the high frequency component amplitude boosted by the dynamic preemphasis circuit to the original amplitude.
This circuit works in the LP and EP modes.

(n) Noise Cancel Circuit
The noise cancel circuit eliminates snow noise remaining in the video signal to produce a video signal with clear edges.

(o) Edge enhancer circuit
This circuit forms a second differentiation type enhancer which emphasizes edges in the picture during playback.

(p) Y/C mixer, clip, buffer circuits
The Y/C mixer mixes the luminance signal output from the edge enhancer and the chroma signal converted to 3.58 MHz.
The mixed signal is passed through the clip and buffer circuits and is output as a playback signal.
This Y/C mixer also works as a squelch circuit.

3) Overview of Chrominance Record Processing Circuit (Fig. 4-21)

Fig. 4-21 shows the main route and processing of the chroma signal in the record mode.

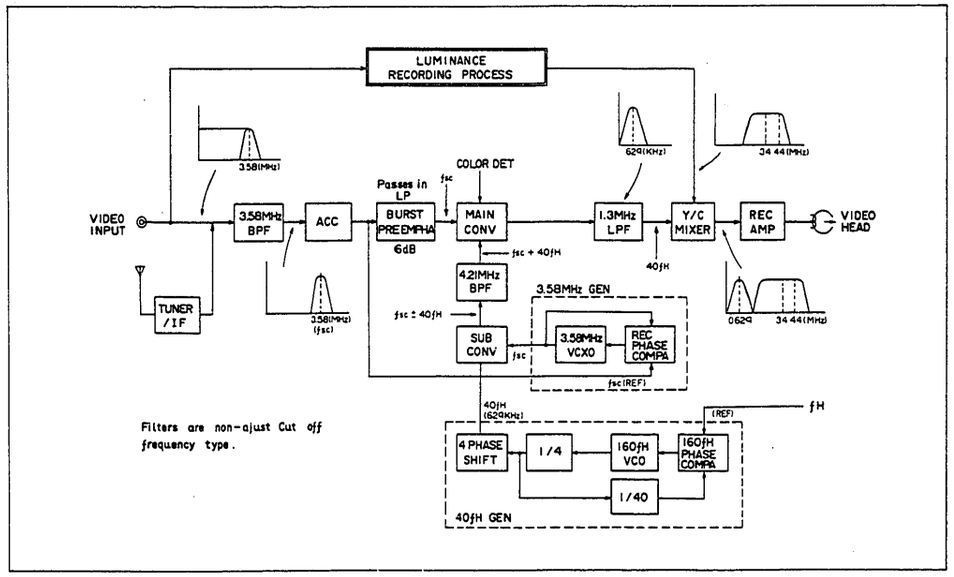


Fig. 4-21 Chroma Record Block Diagram

(a) 3.58 MHz BPF Circuit
The 3.58 MHz bandpass filter circuit selects and passes only the chroma signal (3.58 MHz ± 500 kHz) in the video signal supplied from the video input jack or RF converter circuit.

(b) ACC Circuit
The ACC circuit is provided so that the output level is always constant regardless of input level fluctuations of the chroma signal.

(c) Burst Preemphasis Circuit
The burst preemphasis circuit emphasizes only the burst signal by 6 dB in the SP and EP modes to prevent deterioration of the S/N of the burst signal. In the LP mode, the signal passes this circuit without being controlled.

(d) Record Main Converter Circuit
The record main converter circuit mixes the chroma signal (3.58 MHz ± 500 kHz) fed from the circuit in the previous stage and the precise and stabilized 4.21 MHz carrier signal (fsc + 40 fH) synchronized with the input video signal (H SYNC signal and burst signal). Then it selects the down-converted chroma signal (629 kHz ± 500 kHz) via the 1.3 MHz LPF circuit described later.

(e) 1.3 MHz LPF Circuit
The LPF circuit selects and passes the chroma signal (629 kHz ± 500 kHz) obtained by down-converting the output signal (((3.58 MHz ± 500 kHz)) ± ((3.58 MHz + 629 kHz))) mixed via the record main converter circuit in the previous stage. The chroma signal is adjusted to the optimum level by RT202 and mixed with the FM-modulated luminance signal in the Y/C mixer circuit described in the item "Luminance Record Processing" to become the video recording signal and flows along the same route as described for the luminance signal.

(f) Y/C Mixer / REC Amp Circuit
Same as in Luminance Record Processing Circuit.

(g) 3.58 MHz Generator
The 3.58 GEN circuit during recording oscillates to produce the precise and stable 3.58 MHz signal (fsc) which is synchronized with the burst signal, and this output is sent to the 4.21 MHz sub converter circuit, 3.58 MHz record phase comparator circuit and the color killer detector circuit.

(h) 40fH Generator
During recording the 40fH GEN circuit oscillates the precise and stable 629 kHz signal (40fH) synchronized with the horizontal sync signal, and in addition, this phase advances by 90° every 1H in CH-1 recording, synchronizing with the H.SYNC signal, and in CH-2, it is delayed by 90° every 1H, in reverse. During play, the crosstalk of the chroma signal is removed by reverse processing and making it pass through the 1H delay line.

(i) Sub Converter Circuit
The 4.21 MHz sub converter circuit mixes the output signal (3.58 MHz: fsc) from the 3.58 MHz VCO circuit and the output signal (6.29 kHz: 40 fH) from the 40 fH GEN described previously, and then selects and passes the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal using the next 4.21 MHz BPF circuit, and supplies it to the record main converter circuit.

(j) 4.21 MHz BPF Circuit
The 4.21 MHz BPF circuit selects and passes the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal and then supplies this output to the record main converter.

4) Overview of Chrominance Playback Processing Circuit (Fig. 4-22)

Fig. 4-22 shows the main route and processing of the chroma signal during playback.

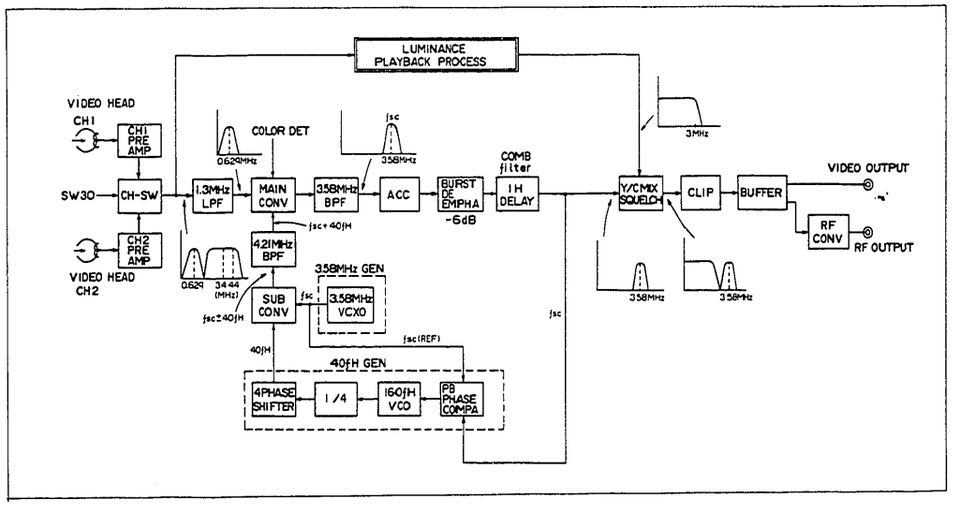


Fig. 4-22 Chrominance Playback Block Diagram

(a) Preamplifier/Channel Switch Circuits
Described previously in "Luminance Playback Processing Circuit".

(b) 1.3 MHz LPF Circuits
The 1.3 MHz LPF circuit selects and passes the chroma signal down-converted to 629 kHz ± 500 kHz from the played back video signal supplied from the channel switch circuit in the previous stage.

(c) Playback Main Converter Circuit
The PB main converter circuit mixes the chroma signal (629 kHz ± 500 kHz) fed from the circuit in the previous stage and the 4.21 MHz carrier (fsc + 40 fH) which is synchronized with the 3.58 MHz crystal oscillator, and then selects the original chroma signal (3.58 MHz ± 500 kHz) via the 3.58 MHz BPF circuit described later. A closed loop is formed among PB MAIN CONV., 3.58 MHz BPF, ACC, BURST

DEEMPHA, 1H DELAY LINE, 40 fH GEN, 4.21 MHz SUB CONV., 3.58 MHz OSC and 4.21 MHz BPF to cancel the frequency variation of the chroma signal caused by the servo fluctuation.

(d) 3.58 MHz BPF Circuit
The 3.58 MHz BPF circuit selects the chroma signal up-converted from the output signal (((629 kHz ± 500 kHz)) ± ((3.58 MHz ± 629 kHz))) of the playback main converter circuit and allows it to pass.

(e) ACC Circuit
Same as in recording.

(f) Burst Deemphasis Circuit
The burst signal is emphasized by 6dB in the SP and EP modes during recording to prevent deterioration of the S/N, so this circuit attenuates it by 6dB in reverse to return the burst signal to its original level.

(g) 1H Delay Line Circuit
The 1H delay line circuit is a filter to eliminate crosstalk in the chroma signal. That is, when the phase of the chroma signal is advanced by 90° every 1H in CH-1 and delayed by 90° every 1H in CH-2 during recording, and it is played back with the crosstalk contained and the phase is returned to the original phase by the reverse process. But the phase of the crosstalk contained in the main signal is reversed every 1H by the reverse process. Then these signals are routed to the 1H delay line which is composed of a direct path and a 1H delay path.
The signals from the delay and the direct paths are added together in the delay line, and the crosstalk components cancel each other because the phases are opposite to each other depending on the paths the signals have passed.

(h) Y/C Mixer/Clip/Buffer Circuit
Same as in Luminance Playback Processing Circuit.

(i) 3.58 MHz VCXO Circuit
The 3.58 MHz VCXO operates as a fixed crystal oscillator during play, generates the precise and stable 3.58 MHz signal, and supplies it to the 4.21 MHz sub converter, color killer detector and PB APC phase comparator.

(j) 40 fH Generator Circuit
The 40 fH GEN circuit produces the 629 kHz which contains frequency variation and phase rotation, to reproduce original chroma signal in the playback main converter. The frequency variation components are needed to cancel frequency fluctuations in the reproduced chroma signal caused by the servo fluctuations. The phase rotation is required for the playback main converter to retrieve the original 3.58 MHz chroma signal which has no phase rotation from the reproduced 629 kHz chroma signal of which the phase changes by 90° every 1H.

(k) 4.21 MHz Sub Converter
The 4.21 MHz sub converter circuit mixes the output signal (3.58 MHz: fsc) from the 3.58 MHz VCXO and output signal (629 kHz: 40 fH) from the 40 fH GEN, and then creates the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal, and supplies it to the 4.21 MHz BPF circuit.

(l) 4.21 MHz Bandpass Filter
Same as in recording.
The 4.21 MHz BPF circuit selects and passes the mixed 4.21 MHz (3.58 MHz + 629 kHz) signal and then supplies this output to the playback main converter.

(3) LUMINANCE RECORDING PROCESS (Fig. 4-33a)

1) General

The luminance recording loop consists of IC201 and IC205 for main controls and peripheral IC202 and IC208. These ICs have been developed for these "1000" series VTRs which use the HQ circuit.

2) Input Select Switch

The line input video or tuner video is selcted by switch IC501 and is supplied to the luminance/ chrominance circuit IC201 via pin 1. This switching is performed by the operator operating the channel select switch (S772/S773) on the front of the VTR. The switching output is applied to IC501 via IC751 (timer μP) and IC801 (tuning μP) to switch IC501.

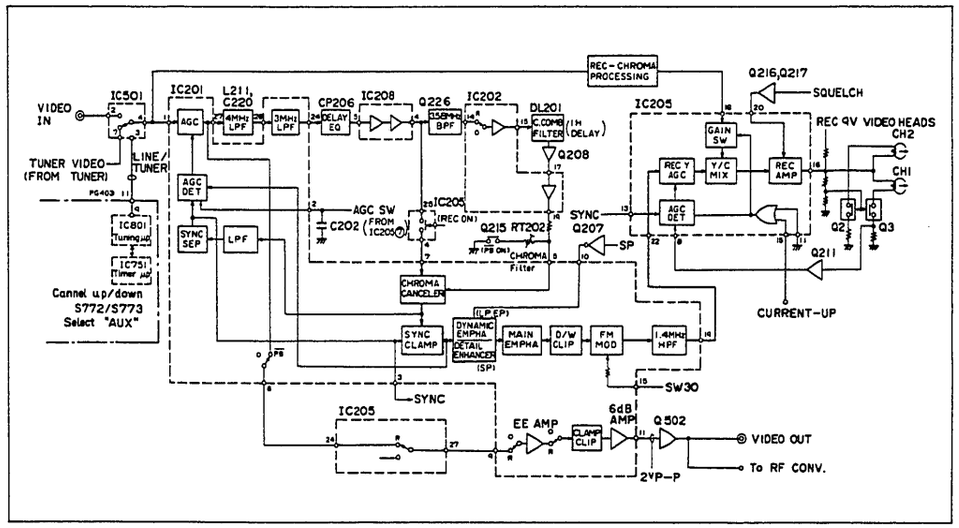


Fig. 4-33a Simplified Luminance Record Circuit

3) AGC (Automatic Gain Control) (Fig. 4-23, 4-24)

The Tuner/IF output video or external input video is selcted by video input selector IC501 and is supplied via pin 1 to the AGC circuit video processing IC201. The AGC circuit is a variable amplifier the gain of which is controlled so the output passing through this circuit is always constsnt (approx. 1 Vp-p) using the detection output of the AGC detector. The AGC detector feeds back the output of the AGC circuit to determine the gain control voltage of the AGC circuit. The video signal fed back to the AGC detector is derived from the output of the chroma canceler and is branched into two circuits. Part is applied to the AGC detector via the clamp circuit. The clamp circuit fixes the sync tip level because the average voltage of the video signal changes according to the picture content. The other is applied to the AGC detector via the lowpass filter (LPF) and sync separator. The LPF filters the video signal and passes only the composite sync signal. The sync separator separates the horizontal sync (H. SYNC) signal from the composite sync signal. The AGC detector delays the H. SYNC signal to the back porch portion, sets the pulse width appropriately and produces a key pulse the voltage of which is determined to 85% white level, then the detector applies the key pulse to the video signal passing through the clamp circuit. Then, the AGC detector detects the peak-to-peak value of the video signal with the key pulse (between the 85% key pulse and sync tip) and charges capacitor C202 at pin 2 with the detected voltage to average it. The voltage charging C202 is applied to the AGC circuit to determine its gain.

The AGC circuit loop described here is the same as in conventional VTRs. However, the AGC circuit in "1000" series VTRs (VT-1100A/1400A) amplifies video signals with a low-luminance level by approx. 15% as shown in Fig. 4-24 to improve the S/N in the low luminance level (the video signal level is less than 1 Vp-p). To do this amplification, the white level of the key pulse is changed to 85% from 100%. Since this causes the control voltage of the AGC circuit to decrease by approx. 15%, the gain is raised by 15%.

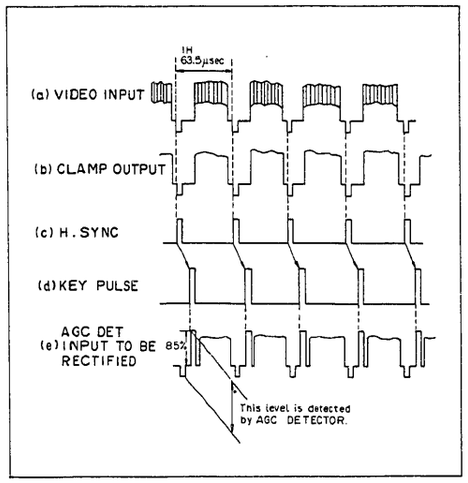


Fig. 4-23 AGC Detector Waveforms

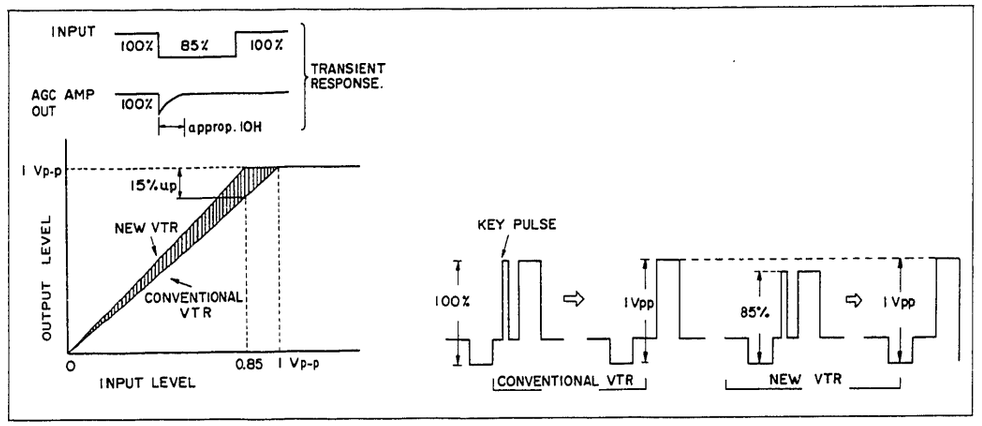


Fig. 4-24 AGC Characteristics

4) Luminance Separation Circuit (Fig. 4-25, 4-26)

This circuit separates the luminance signal using an LPF and comb filter (1H Delay Line). The signal at the AGC output (IC201 pin 27) with the luminance and chrominance components mixed is passed through two stages of the LPF and almost only the luminance signal is derived. However, since this luminance signal contains a little of the chroma component (approx. -15 dB), the remaining chroma is eliminated by the chroma canceler in the next stage. (See Fig. 4-26 for details.) The delay equalizer in Fig. 4-25 not only delays the signal to correspond to the delay in the chroma signal processing loop but compensates the phase chracteristics of the two LPFs. Fig. 4-26 shows the operation of the chroma canceler circuit. The input video signal (A) contains the mixed luminance and chroma components. (Actaully, the chroma

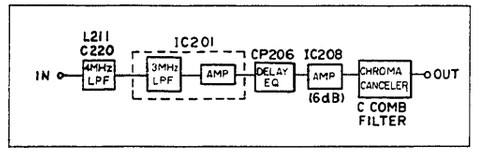


Fig. 4-25 Luminance Separation Circuit

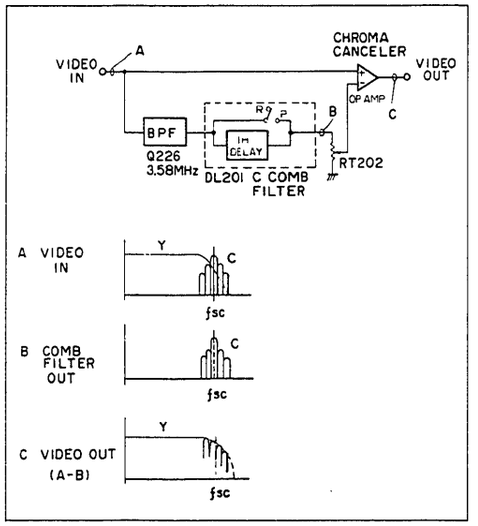


Fig. 4-26 Chroma Canceler Circuit

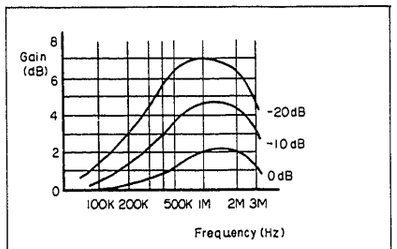
level is lower than the luminance level, but it is described at the same level as the luminance level so it can be seen more easily.)
The chroma signal (3.58 ±1 MHz) passing through the BPF enters C COMB filter DL201. The input signal is added to the signal passing through the 1H delay circuit. Only the chroma signal is derived at the comb filter output (B) and it is subtracted from the original signal at the operational amplifier (chroma canceler in IC201) and only the luminance signal after the chroma signal is eliminated appears at the output as shown by (C).
RT202 in the former stage of the chroma canceler is a variable resistor which balances the input level of OP AMP 2. The chroma canceler circuit acts the same as the 3.58 MHz trap in "60" series VTRs and before. This expands the frequency response of the luminance signal (approx. 3 dB up at 3 MHz) and reduces the crosstalk of the chroma signal more than in previous VTRs.

5) Sync Clamp Circuit

Since the DC component of the video signal is not supplied through capacitors, the sync tip level of a bright picture is not the same as the sync tip level of a dark picture. For the FM modulator, it is necessary to equalize the sync tip levels. This circuit equalizes the sync tip levels. The output of the clamp circuit is sent to the emphasis circuit.

6) Dynamic Preemphasis Circuit (Fig. 4-27)

The dynamic (nonlinear) preemphasis circuit performs the emphasis operation shown in Fig. 4-27 corresponding to the video signal input level and tape speed. This selection of the emphasis characteristic at each tape speed is performed by applying "SP Lo" to IC201 pin 10.
The output of the dynamic (nonlinear) emphasis circuit is supplied to the main preemphasis circuit.



LP and EP Mode
(Works as detail enhancer in SP mode)

Fig. 4-27 Dynamic Emphasis

7) Detail Enhancer

This circuit is the result of HQ technology and operates in place of dynamic emphasis in the SP mode. (See "VHS HQ SYSTEM" for details.)

8) Main Preemphasis Circuit (Fig. 4-28)

The dynamically emphasized luminance signal is now supplied to the main preemphasis circuit where the high-frequency components of the signal are boosted more than the low-frequency components. The frequency response for the preemphasis is shown in Fig. 4-28. The boosting action is required for the high-frequency components because in the FM recording system, the noise of the playback signal increases in proportion to the modulated signal frequency. In the playback process, the emphasized signal is deemphasized to resume the original signal. By the dynamic emphasis and the main preemphasis operation, the total S/N ratio increases.

The output of the main preemphasis circuit is supplied to the dark and white clip circuit.

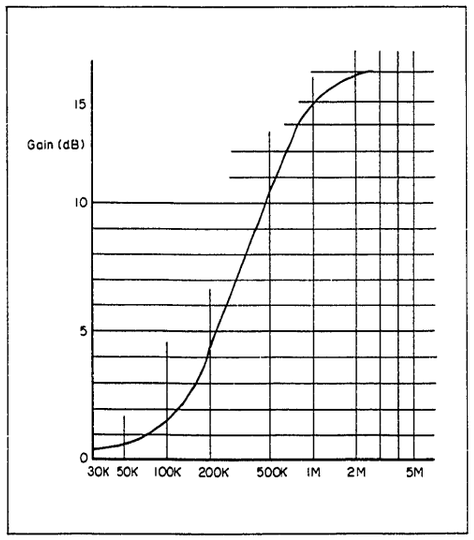


Fig. 4-28 Preemphasis

9) Dark and White Clip Circuit (Fig. 4-29)

After emphasis is performed, any unusually large overshoots and undershoots in the luminance signal are cut off at an specified level. This is done to avoid FM over-modulation. The overshoot levels are controlled by the white clip circuit and the undershoot levels are controlled by the dark clip circuit. Every clip level has been adjusted to the optimum value in IC201. The output of the dark and white clip circuit is supplied to the FM modulator circuit. The head switching pulse is added to this output to apply FM interleaving.

The white clip level is increased by approx. 20% by one HQ technology.

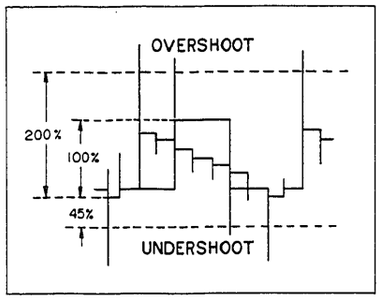


Fig. 4-29 Dark/White Clip

10) FM interleaving

The video signal of the adjacent channel is recorded overlapping the main channel. When recording/play is done as it is, beats occur between the main channel and adjacent channels, so CH1 is left as it is and only for CH2 the carrier frequency of the FM modulator is lowered by 1/2 fH. The head switching pulse (SW30) is applied to the video input main line of the FM modulator from the servo circuit via IC201 pin 15. By this, the carrier frequency drifts by 1/2 fH when SW30 is "Hi" (CH2).

11) FM Modulator Circuit (Fig. 4-30)

The actual device which constitutes the FM modulator is an astable multivibrator. This multivibrator generates a variable frequency square wave. The frequency of the square wave is governed by the level of the processed video signal at any given moment. Therefore, the processed signal varies the frequency of the square wave, which is frequency modulation, or FM.

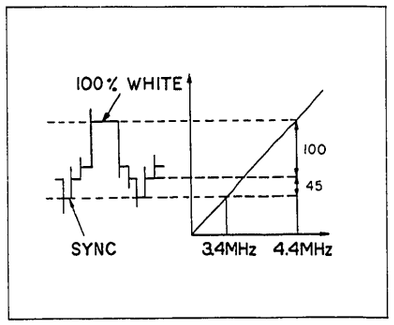


Fig. 4-30 FM Modulation

12) 1.4 MHz HPF Circuit (Fig. 4-31)

When the carrier of the FM modulator swings from 3.4 MHz to 4.4 MHz, sidebands are also produced. The lower sideband extends down to (and below) 500 kHz. When recording the chroma signal, the lower FM sideband must be removed to prevent chroma beats during playback.

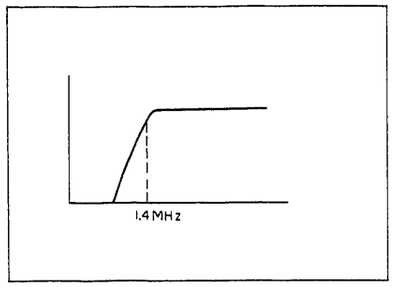


Fig. 4-31 Band Response of HPF

13) Y/C Mixer and Recording Amplifier (Fig. 4-32)

The FM-modulated luminance signal and the chroma signal, the frequency of which is down-converted (to 629 kHz) by the chroma processing circuit, are mixed by the Y/C mixer and the mixed signal is amplified by the recording amplifier to be the specified level and is then supplied to the video heads. Pin 20 of IC205 inhibits recording.
When pin 20 goes "Hi" (SQUELCH signal "Hi"), it stops the operation of the recording amplifier to inhibit recording. The SQUELCH signal is "Hi" during loading (for approx. 2.5 seconds), pause and phase match edit operation (for approx. 1.2 seconds).

Transistors Q2 and Q3 turn "on" receiving REC 9V in the record mode and ground one end of the winding of the video head (actually, the winding of the rotary transformer) via the resistor with low resistance (10 ohms).

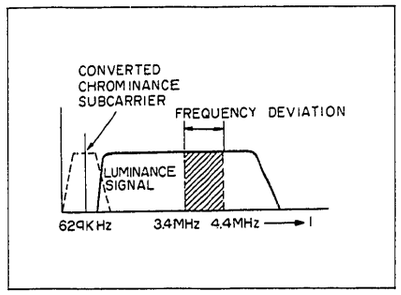


Fig. 4-32 Spectrum of FM Signal

14) Recording AGC Circuit (Fig. 4-32a)

The FM recording current flowing to the video heads must be aligned with the optimum recording current matching the characteristics of the video heads. In conventional VTRs (until "60" series VTRs), this was adjusted by an externally attached control, however, in "1000" series VTRs, by employing the recording AGC, no adjustment is required.

Fig. 4-32a shows the operation of this circuit. The FM signal enters IC205 via pin 22 and passes through the AGC amplifier (gain control amp), Y/C mixer and the recording amplifier and is then supplied to the video heads via pin 16. The voltage across resistor R5 (10 ohms) is changed by the recording current level. This change component is amplified by Q211 and enters IC205 via pin 8 and passes through the amplifier and OP AMP and is then fed back to the AGC amplifier. If the recording current is large, the voltage across R5 becomes high and the voltage at pin 8 is high. This lowers the gain of the AGC amplifier to control it so the recording current becomes constant.
IC205 pin 13 is the SYNC input which closes the switch only the sync signal is present to form an AGC loop. This eliminates the affect of fluctuations in the chroma signal which is superimposed in the Y/C mixer.
The output at pin 28 (CURRENT UP) of system control microprocessor IC901 is connected to pin 15 of IC205. This output increases the recording current for the time of overlap-recording on the tape (for approx. 3 seconds) and improves the picture quality (reduction of chroma beats) in the overlap-recorded section.

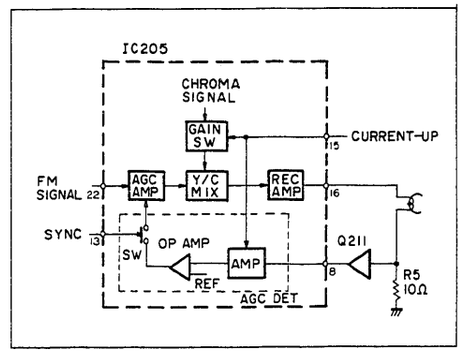


Fig. 4-32a Recording AGC Circuit

15) E-E Monitor Circuit

Part of the AGC output is derived from IC201 pin 8 as an E-E monitor signal. The monitor signal from pin

8 is supplied to IC205 pin 24 and is directly output at pin 27. This output is applied to pin 9 of IC201 and is clipped by the clip circuit so the white peak is 125% and is then amplified and output from pin 11 with the level of approx. 2 Vp-p. This output is converted by Q502 on the main P.C.B to low impedance and is applied to the video output jack and RF converter.

16) Luminance Filter (Fig. 4-33)

A new system is employed to comprise three filters in IC201 - a 3 MHz LPF, an LPF for sync separation and a 1.4 MHz HPF so no ajustment is required when manufacturing ICs in the factory.
It is very difficult to suppress variations in elements (resistance values of resistors and capacitances of capacitors) when manufacturing ICs. However, even though the variations of the absolute values are great, the variations of the relative values between the elements are small (this is called a high relative accuracy). Using this fact, a new system with three filters has been designed. The operation principle is shown in Fig. 4-33.
The input reference frequency (2fsc) signal is attenuated to a specified level by resistors Ra and Rb with high relative accuracy to become a reference level. This reference level and the output level of a quasi-filter consisting of integrated elements R1 and C1 are compared in the operational amplifier, and negative feedback is applied to the voltage applied to varicap C1 so both levels are aligned.

Meantime, using elements R2 - R4 and C2 - C4 which are related to the quasi-filter elements R1 and C1 with high-relative accurcy, the necessary filters are provided.
When variations occur in the values of the integrated elements (R1/C1) and this causes the quasi-filter output level to fluctuate between points A and C as shown in Fig. 4-33, the automatic adjustment function works to control the varicap C1 so point B can be obtained.
Since this control voltage applied to C2 - C4, the respective LPFs and HPF are adjusted to the required frequencies with high precision.

Fig. 4-33 Filter Principle Diagram (Luminance)

(4) LUMINANCE PLAYBACK PROCESS (Fig. 4-37a)

1) General

The luminance playback loop consists of IC201 and IC205 at the center and IC204/IC207/IC208 on the luminance/chroma P.C.B and IC1 on the preamplifier P.C.B connected directly to the cylinder.

2) CH1 and CH2 Preamplifier Circuits

The Playback signals input to IC1 pins 12 and 14 are fed to the CH1 and CH2 preamplifier circuits. The preamplifier circuits feed back the output signal to the input side to make the characteristics flat. The conventional play equalization is performed via the 4.6 MHz peaking circuit (CP203) provided after the channel switch circuit.

Q1 is turned "on" by the PB 5V power source and grounds one end of the windings of the CH1 and CH2 video heads. The STILL head has the same azimuth as the CH2 head. The CH1 head is switched to the STILL head by the STILL signal input to pin 3 of IC1 in the still play mode.

3) Channel Switch Circuit

The channel switch circuit produces a continuous playback signal while switching the outputs of CH-1 and CH-2 preamplifier circuits using the head switching pulse (SW30).
The head switching pulse (SW30) generated in the servo circuit is supplied to the channel switch circuit via IC1 pin 4, and selects the output of CH-1 preamplifier which amplifies the video signal picked up by the CH-1 video head when the head switching pulse level is set to "Lo", and selects the output of the CH-2 preamplifier which amplifies the video signal picked up by the CH-2 video head when the pulse level is set to "Hi".

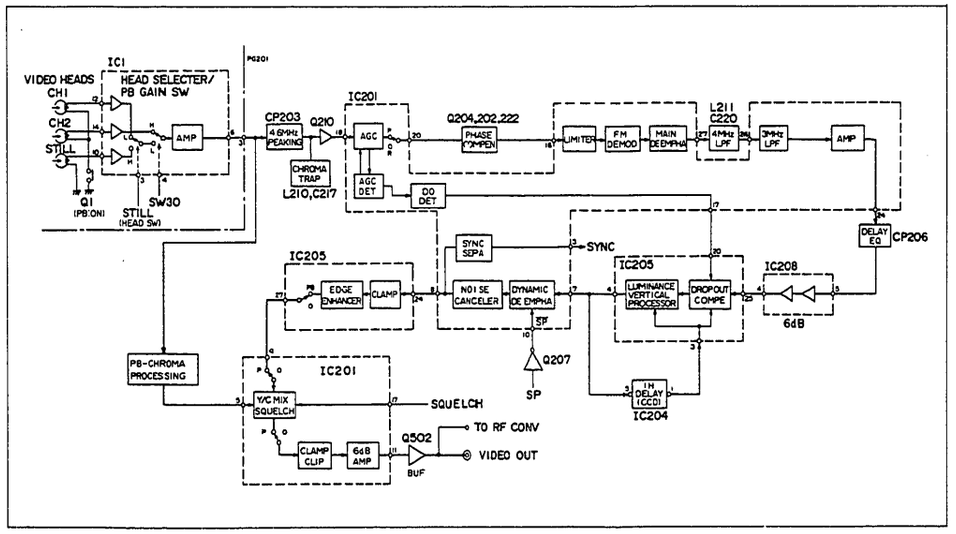


Fig. 4-37a Simplified Luminance Playback Circuit

The output of the channel switch circuit is applied to the 4.6 MHz peaking circuit via amplifier and IC1 pin 6.

4) 4.6 MHz Peaking Circuit, Chroma Trap Circuit (Fig. 4-34)

The preamplifier circuit in the previous stage does not apply playback compensation to the signal and has flat characteristics, so the 4.6 MHz peaking circuit performs playback compensation. The playback characteristics of the video signal picked up by the CH-1 and CH-2 video heads are as shown by curve (A) in Fig. 4-34.

The characteristics of the preamplifier circuit are as shown by curve (B) and are flat. The characteristics of the 4.6 MHz peaking circuit (CP203) should be made as shown by curve (D) so that the integrated characteristics shown by curve (C) are obtained finally.

Components around the 4.6 MHz which is the upper limit of the FM carrier signal are boosted by the 4.6 MHz peaking circuit (CP203) to obtain the characteristics shown by curve (D).

The output of the 4.6 MHz peaking circuit is supplied to the AGC circuit via 629 kHz (chroma) trap, buffer and IC201 pin 18.

The 629 kHz (chroma) trap circuit (L210, C217) eliminates the 629 kHz playback chroma components.
Q210 is a buffer amplifier to change the impedance.

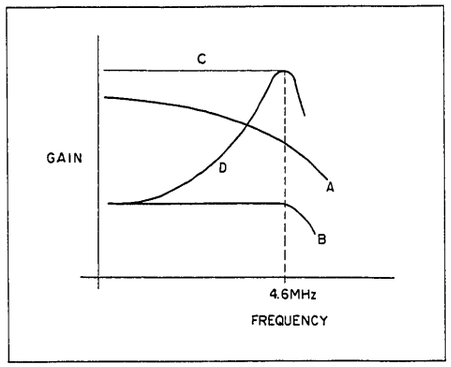


Fig. 4-34 Frequency Characteristics

5) AGC Circuit

The output from the 4.6 MHz peaking circuit is applied to the AGC amplifier stage where the RF output (FM) signals from the two video heads are automatically balanced.

One of the AGC circuit outputs is fed to the AGC detector circuit which detects signal level fluctuations. This is fed back to the AGC circuit to control so that the AGC circuit output is constant.

The AGC circuit output is derived from pin 20 of IC201 and is applied to the phase compensator circuit in the next stage. The other AGC circuit output is applied to the dropout detector circuit to detect missing of the FM signal due to dust or dirt on the tape, poor or irregular tape coating, etc. The detected output is derived from IC201 pin 17 which goes "Hi" when the FM signal is missing.

6) Phase Compensator Circuit (Q204, Q202, Q222)

The phase compensator circuit (Q204, Q202, Q222) corrects the phase distortion occurring in the 4.6 MHz peaking circuit (CP203) described previously.

The output of the phase compensator circuit is supplied to the FM demodulator circuit via IC201 pin 16 and highpass limiter circuit.

7) Limiter Circuit

The limiter circuit removes amplitude variations in the FM signal. The limiter also limits the amplitude of the FM signal after boosting the FM high-frequency components to prevent black and white from being inverted. That is, the FM carrier output level becomes smaller than the low-frequency sideband level in the high modulation section of the played back FM signal causing distortion; when it is demodulated via the FM demodulator as it is, black/white inversion occurs.
The limiter circuit prevents this.

8) FM Demodulator Circuit (Fig. 4-35)

This circuit uses the pulse delay system.
The FM demodulator circuit first converts the FM signal to a pulse the duty cycle of which is inversely proportional to the input FM signal frequency, that is, converts the FM signal to a pulse-width-modulated signal. Then the circuit smooths this PWM signal to demodulate the video signal.

The output of the FM demodulator circuit is applied to the main deemphasis circuit.

Fig. 4-35 shows the demodulator characteristics.

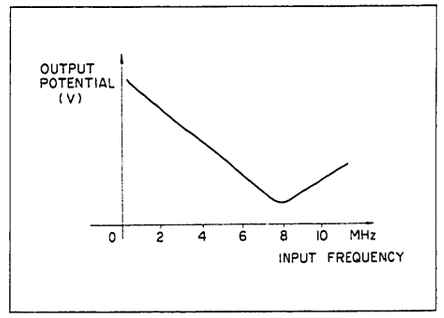


Fig. 4-35 Demodulator Characteristics

9) Main Deemphasis Circuit

The main deemphasis circuit attenuates the high frequency component, boosted by the main preemphasis circuit during recording, during play. That is, this circuit returns the high frequency component amplitude emphasized during recording to the original value.

The output from the main deemphasis circuit is sent to the 4 MHz LPF circuit via IC201 pin 27.

10) LPF Circuit, Delay Equalizer

The LPF circuit (4 MHz LPF + 3 MHz LPF) passes only the luminance signal of 3 MHz or less and the delay circuit (CP206) corrects the phase difference between the luminance signal and chroma signal.

The output of the AGC circuit also flows to this circuit during recording, and the same processing with the same characteristic is performed in the record and play modes.

11) Amplifier Circuit (IC208)

This circuit is between the output of delay equalizer and the dropout compensator circuit in the next stage and is an amplifier the gain of which is approx. 6 dB.

12) Dropout Compensator Circuit (Fig. 4-36)

This circuit compensates for missing parts of the FM signal due to dust or dirt on the tape, irregular tape coating, etc. and is used in common with the vertical processor circuit. Fig. 4-36 shows the dropout compensator circuit. (Compare this with Fig. 4-15 for easy understanding.)

The dropout detection output detected by IC201 is derived from pin 17 and is applied to pin 20 of IC205. The video signal input to pin 25 passes through SW1 and OP AMP 2 and is output from pin 4 normally. The 1H delay circuit (IC204) using a CCD is connected to the output at pin 4, and the output is fed back to pin 3 and is connected to the other terminal (b) of SW1. That is, the video signal 1H before the signal at terminal (a) is always supplied to the terminal (b). If missing parts of the FM signal (dropout) occur, IC205 pin 20 goes "Hi" and the contact of SW1 is switched to (b), so the output can be compensated by the signal 1H before while dropout occurs.

In conventional VTRs, dropout is compensated before FM demodulation, that is, in the FM signal stage. This dropout compensation system in the video signal circuit which is used from "1000" series VTRs can reduce switching noise.

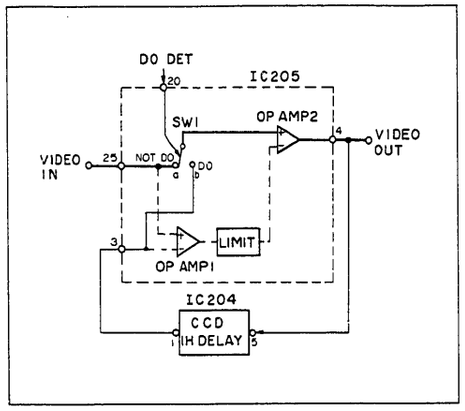


Fig. 4-36 Dropout Compensation Circuit

13) Luminance Vertical Processor

This circuit has been developed as one HQ technology to improve the S/N.

14) CCD 1H Delay Circuit (Fig. 4-36a)

This circuit consists of a hybrid IC in which a monolithic integrated circuit with 1H delay function using a CCD (Charge Coupled Device) and two externally attached LPFs. The clock frequency driving the monolithic IC is designed to be 2fsc.

The fsc (3.58 MHz), output from pin 41 of IC202, is applied to IC204 via pin 14 and is passed through the multiplier circuit (X2, 2fsc BPF) to produce 2fsc. This 2fsc is applied to the monolithic IC via the buffer amplifier to drive it.

Describing the signal flow, the video signal enters IC204 via pin 5 and is sampled at the period of 2fsc by the sampling circuit. The sampled pulse (455 bits per 1H) is 1H-delayed by the CCD in the next stage and is returned to an analog signal by the resampling circuit. CP204 is a lowpass filter which eliminates the clock frequency (2fsc). The LPF output is applied to pin 1 via the buffer amplifier.

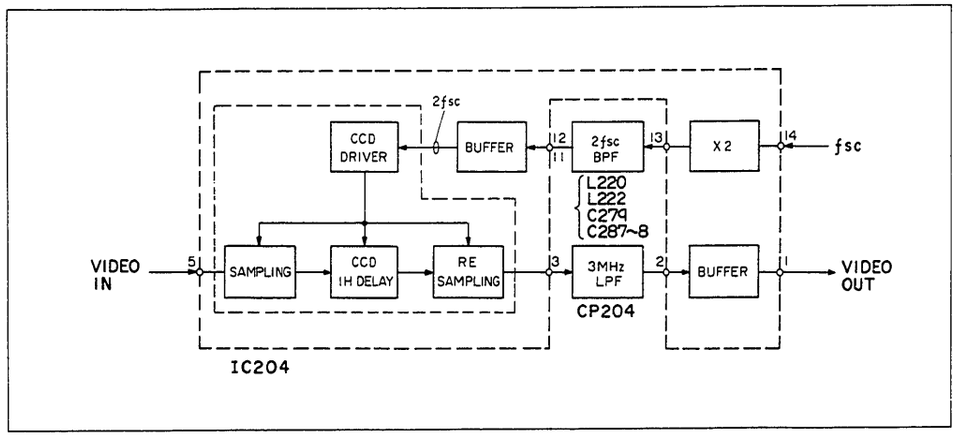


Fig. 4-36a CCD 1H Delay Circuit

15) Dynamic Deemphasis Circuit

This circuit forms a counterpart to the dynamic preemphasis circuit during recording. The characteristics are also reverse to those in recording. This circuit is activated by the $\overline{SP}$ signal at pin 10 of IC201.

16) Noise Cancel Circuit

The noise cancel circuit almost completely removes the high-frequency noise contained in the video signal which has passed through the dynamic deemphasis circuit.

The output of the noise cancel circuit is supplied to the clamp circuit via IC201 pin 8 and IC205 pin 24. The clamp circuit fixes the sync tip voltage of the video signal and applies it to the edge enhancer circuit in the next stage.

17) Edge Enhancer Circuit (Fig. 4-37)

This circuit emphasizes the edges of the picture and uses the second differential circuit as shown in Fig. 4-37.

The description assumes that a square wave as shown in (A) is applied to the input. The leading edge of the LPF output waveform is shallow as shown in (B). The other signal is supplied to the second differential circuit after its sync signal is eliminated. When the signal is differentiated once by the scond differential circuit, the differentiated waveform as shown in (C) is obtained and the signal is differentiated again, the second differentiated waveform appears as shown in (D). When this differentiated signal is controlled by the gain control circuit in the next stage to be set to the appropriate level and is subtracted from the signal (B) by the OP AMP, the waveform with its edges emphasized appears at the final output (E).
The gain of the gain control amplifier is controlled by the voltage at IC205 pin 23 to determine the amount of emphasis of the edges.

18) Y/C Mixer Circuit, Squelch Circuit

The Y/C mixer circuit mixes the luminance signal and the chroma signal supplied from IC201 pin 5. This circuit also has a squelch function.

The squelch circuit outputs a DC potential of which level is the same as sync-tip to black out the screen while pin 17 is "Hi". During loading, pin 17 is given a high potential, and the squelch circuit cuts the playback video signal. In the trick play mode, when a positive pulse "ARTIFICIAL V.SYNC" of which pulse width is approx. 8H is applied to pin 17, the squelch circuit outputs the sync tip level potential to add the artificial V.sync to the playback video signal. The potential of pin 17 is supplied from the servo circuit.

The output of the Y/C mixer circuit is applied to the clamp circuit. The signal route thereafter is the same as that described in "LUMINANCE RECORDING PROCESS".

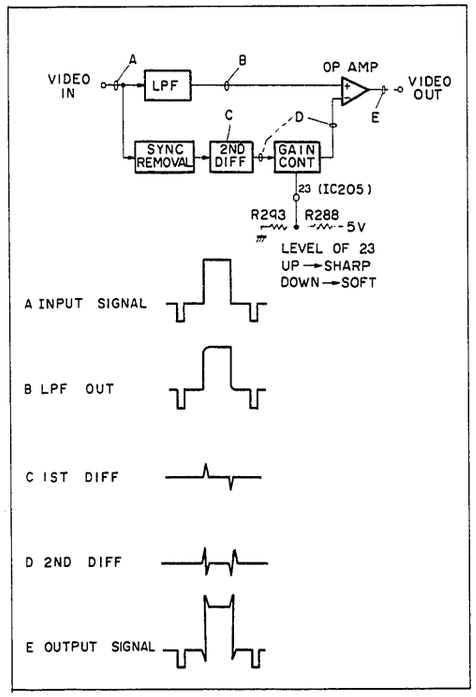


Fig. 4-37 Edge Enhancer

(5) CHROMINANCE RECORDING PROCESS (Fig. 4-43a)

1) General

The chroma signal during recording is processed by IC202 in the luminance/chroma P.C.B. IC202 performs the chroma signal processing during play, the same as for the luminance signal, so it is required to switch over the signal routes. The switching command is given by the "PB5V" signal supplied via pin 18. This level is set to "Lo" during recording and the SW inside IC202 is set to the "PB" position and the signal route during recording is formed. Next, every circuit operation is described in order of the signal route as follows.

2) PB/$\overline{PB}$ SW

The video signal fed from the video input jack is supplied to the PB/$\overline{PB}$ switch via IC202 pin 25. The route from the 3.58 MHz BPF circuit (CP202) until the ACC circuit in IC202 is commonly used for recording and play, so the PB/$\overline{PB}$ SW circuit selects the signal input to this circuit. The PB/$\overline{PB}$ SW circuit is controlled by the PB5V signal fed from pin 18; this signal is set to "Lo" during recording, and the video signal at pin 25 is supplied to the 3.58 MHz PBF circuit via the PB/$\overline{PB}$ SW circuit and pin 23.

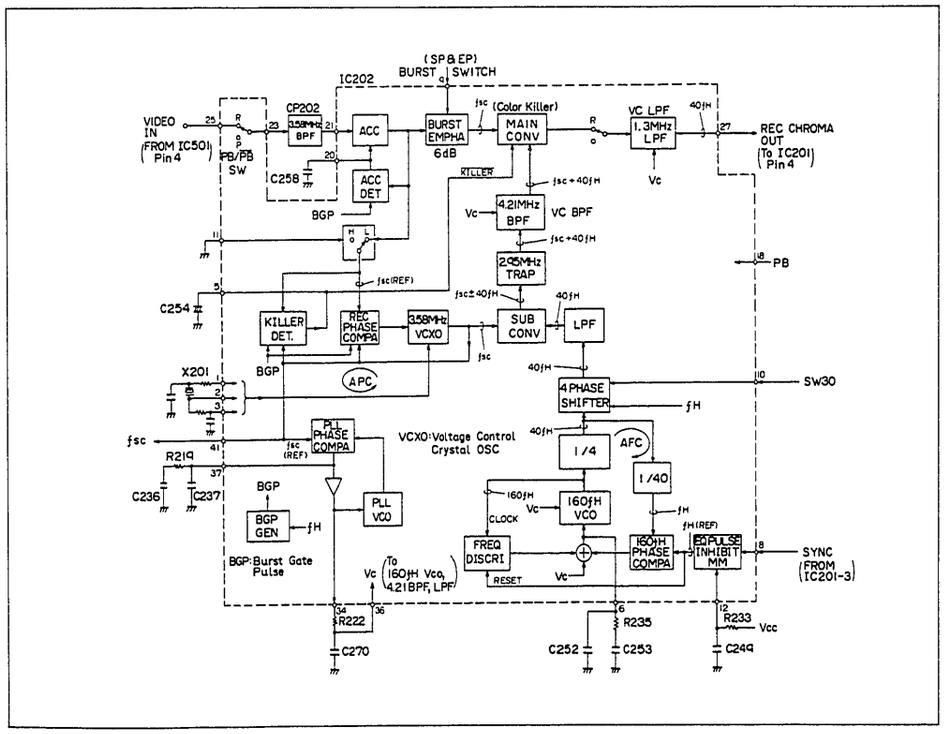


Fig. 4-43a Simplified Chrominance Record Circuit

3) 3.58 MHz Bandpass Filter Circuit

The 3.58 MHz bandpass filter circuit (CP202) selects only the chroma frequency band (3.58 MHz ± 500 kHz) from the input video signal and passes it.

The output of the BPF circuit is supplied to the ACC circuit via IC202 pin 21.

4) ACC (Automatic Color Gain Control) Circuit (Fig. 4-38)

The ACC circuit controls the output level to a constant value regardless of fluctuations of the chroma signal input level.

This control system is the burst ACC system. First, the ACC circuit output is supplied to the ACC detector circuit. Then the ACC detector circuit receives the burst gate pulse. The ACC detector circuit extracts the chroma burst signal by means of these 2 signals and detects the burst signal level. This charges C258 connected to pin 20 and is averaged. This voltage is fed back to the ACC circuit, and by this, the gain is controlled so that the output voltage of the ACC circuit is constant.

The output of the ACC circuit is fed to the burst preemphasis circuit.

The H.SYNC gate eliminates the equalizing pulse contained in the H.SYNC signal sent from IC202 pin 8, and triggers the burst gate pulse generator every 1H. The burst gate pulse is delayed from the H.SYNC signal so that only the burst signal is gated from the chroma signal, and moreover, it is provided with the pulse width of the burst signal period. (Refer to Fig. 4-38)

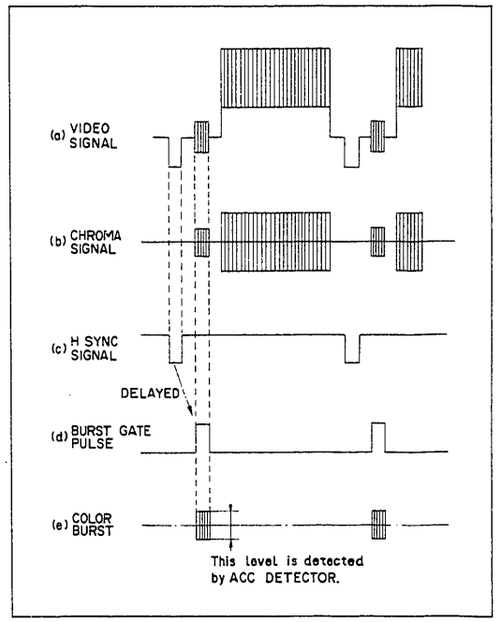


Fig. 4-38 ACC

5) Burst Preemphasis Circuit (Fig. 4-39)

The burst preemphasis circuit amplifies only the chroma burst signal by 6 dB using the burst gate pulse in the SP and EP modes.
IC202 pin 9 is "Lo" in the LP mode, the burst gate pulse switch is "off" and the burst preemphasis function does not work. The output of the burst preemphasis circuit is transmitted to the record main converter circuit in the next stage.

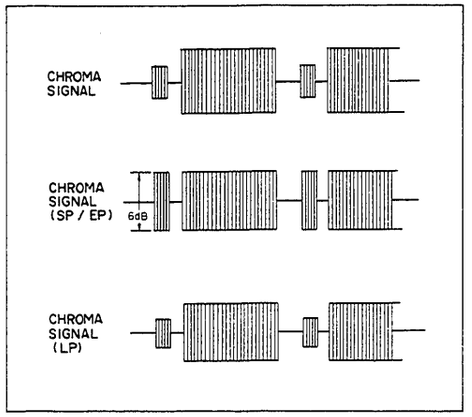


Fig. 4-39 Burst Preemphasis

6) Record Main Converter Circuit (Fig. 4-40)

The purpose of this record main converter is to produce a 629 kHz chroma signal with phase rotation.

This means that the second input to this main converter must have phase rotation, and must be such a frequency that the difference between the two input frequencies is the desired output frequency. Therefore, the second input is a 4.21 MHz rotational signal. The 4.21 MHz signal is a continuous sinewave signal which is phase-locked to the input horizontal sync.

The 4.21 MHz signal will change its phase by 90° every time a new horizontal sync signal is received. Because one of the inputs to the main converter has a phase rotational characteristic, the output signal will also have the same characteristic.
The output contains two bands of information. It contains the sum and difference frequency components of the two input signal frequencies.
The sum is the 7.8 MHz rotational chroma signal.
The difference is the necessary 629 kHz rotational chroma signal.
The output of the record main converter circuit is fed to the 1.3 MHz LPF in the next stage.

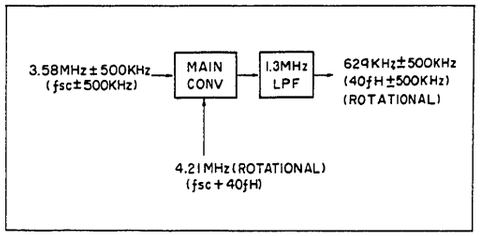


Fig. 4-40 Record Main Converter

7) Color Killer Detector Circuit

The killer detector circuit controls the record color killer so that the chroma signal is allowed to pass only when the chroma burst signal is contained in the video signal. The presence/absence of the chroma burst signal is detected by the color killer detector circuit. The color killer detector circuit inputs the following 3 signals and performs sync-detection to detect presence/absence of the chroma burst signal.

(1) Chroma signal:
This signal is supplied from the input side of the burst preemphasis circuit.

(2) Burst gate pulse:
This signal is produced in the burst gate pulse generator.

(3) 3.58 MHz signal:
This signal is supplied from the 3.58 MHz VCXO (Voltage Controlled Crystal Oscillator) and sync-detected with the chroma burst signal to detect the presence/absence of the burst signal.

The output of the killer detector circuit charges C254 connected to pin 5 where it is averaged and supplied to the record main converter (has a color killer function); this level is set to "Lo" when the chroma burst signal is present, and to "Hi" when the chroma burst signal is not present.

8) 1.3 MHz Lowpass Filter Circuit

The 1.3 MHz LPF circuit cuts off the sum component - 7.8 MHz rotational chroma signal - from the output of the record main converter circuit and selects only the difference component - 629 kHz rotational chroma signal - and passes it.

The output of the LPF is applied to the Y/C mixer circuit via IC205 pin 18 and mixed with the luminance signal. The signal route thereafter is the same as described in the item, "LUMINANCE RECORDING PROCESS".

9) Derivation of 4.21 MHz Rotational Signal

The 4.21 MHz rotational signal is generated in IC202. Since the 4.21 MHz signal is phase-locked to the incoming video signal, two comparator circuits, AFC and APC, are used as phase-locked loops. In brief, the AFC circuit produces a 160 fH (2.571 MHz) signal which is counted down and converted to a 629 kHz rotational signal. The APC circuit generates a 3.58 MHz signal which, when multiplied by the 629 kHz rotational signal inside a 4.21 MHz sub converter, will produce the desired 4.21 MHz rotational signal. This simplified description can be seen below. The AFC circuit locks to the incoming horizontal sync signal, and produces a 160 fH output signal. This signal is supplied to the 1/4 divider and then to the 4 phase shifter circuit which produces a 629 kHz rotational signal.

Again, "rotational" indicates a phase change of 90° per horizontal line. The APC circuit locks to the incoming burst signal and produces a continuous 3.58 MHz output signal. The 629 kHz rotational signal and the 3.58 MHz signal are combined in 4.21 MHz sub converter, and the output is a 4.21 MHz rotational signal. This 4.21 MHz rotational signal is the signal that is used in record main converter inside of IC202.

10) Recording AFC Circuit

The REC. AFC is composed of mainly the 160 fH VCO circuit, 1/4 divider, 1/40 divider and the record 160 fH phase comparator circuit. The 1/4 and 1/40 dividers divide the 2.517 MHz signal generated by the 160 fH VCO down to 15.734 kHz. The 15.734 kHz signal is supplied to the 160 fH phase comparator circuit.

The other input to the record 160 fH phase comparator is the H.SYNC pulse which is derived from the incoming video signal. Therefore, the 629 kHz signal is phase locked to the incoming video signal. The output of the record 160 fH phase comparator circuit is charged to C252/C253 connected to pin 6 and is averaged. Then this DC voltage is fed back to the 160 fH VCO circuit.

If the fH signal from the counted down 629 kHz signal does not phase-match the incoming horizontal sync, an error voltage will be generated and applied to the VCO so that phase matching does occur.

When the 160 fH VCO is providing the proper phase-locked 2.517 MHz signal, the 4 phase shifter outputs the 629 kHz rotational signal.

11) 4 Phase Shifter (Fig. 4-41, 4-42)

The 1/4 divider circuit divides the 160 fH (2.517 MHz) by 4 and supplies four 629 kHz pulses with different phases to the 4-phase shifter. The 4-phase shifter generates the phases rotational 629 kHz using 629 kHz signals and 4 enabling signals. Fig. 4-41 is the equivalent block diagram of the 4-phase shifter. The AND gates are fired in order to provide a phase rotating output. The enabling signals can be obtained by applying the H.sync pulse selected by the H.sync gate circuit to the ring counter. The phases of the enabling signals are changed by the level of the SW30Hz signal applied via pin 10. Fig. 4-42 shows the phases of the enabling signals.

For the first field for video head "CH1" the firing order of gates is 1-2-3-4. This provides the desired 0°, 90°, 180°, 270°, etc. rotation.

For the second field for video head "CH2", the order is 1-4-3-2. This gives a 0°, 270°, 180°, 90° rotation, which is the same thing as 0°, minus 90°, minus 180°, minus 270° rotation, which is desired.

When the SW30 signal is set to "Lo", the 629 kHz signal with the phase 90° advanced every cycle of the fH signal is selected and when the SW30 signal is set to "Hi", the 629 kHz signal with the phase 90° delayed every cycle of the fH signal is selected. This control is processed digitally.

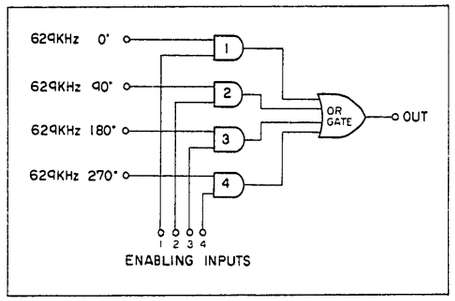


Fig. 4-41 4-Phase Shifter

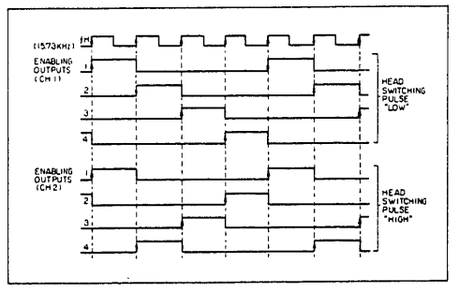


Fig. 4-42 Enabling for 4-Phase Shifter Gates

12) 3.58 MHz Generator

The 3.58 MHz GEN mainly consists of the 3.58 MHz VCXO and the record 3.58 MHz phase comparator. When recording, this circuit derives the chroma burst signal and locks the oscillation frequency of the 3.58 MHz VXCO to the frequency of this derived burst signal, then applies this output to the 4.21 MHz sub converter and the color killer detector circuits.

The 3.58 MHz VCXO circuit generates the 3.58 MHz signal while synchronized with the chroma burst signal.
The record 3.58 MHz phase comparator circuit inputs the following 3 signals and locks the 3.58 MHz VXCO oscillation frequency to the chroma burst signal frequency.

(1) 3.58 MHz signal:
This signal is supplied from the 3.58 MHz VCXO circuit.

(2) Chroma burst signal:
This signal is derived from the chroma signal output from the burst preemphasis circuit described previously using the burst gate signal.

(3) Burst gate pulse:
This signal is produced in the burst gate pulse generator.

The output of the phase comparator circuit charges C235 connected to pin 38 and is fed back to the 3.58 MHz VCXO circuit.

13) Chrominance Filter (Fig. 4-43)

These three circuits, 160fH VCO, 4.21 MHz BPF and 1.3 MHz LPF, in IC202 operate using a PLL VCO as a link so no adjustment is required when manufacturing ICs.

a) Using the 3.58 MHz VCXO output signal fsc as a reference signal and the PLL VCO output signal (3.58 MHz) as a comparison signal, both phases are compared by the PLL phase comparator and the error signal is fed back to the PLL VCO via the LPF and DC amplifier.

b) The feedback voltage (PLL control voltage) is reapplied via pin 36 to IC202 through the externally attached LPF. (Control voltage Vc)

c) This control voltage is applied to the VCO, LPF and the variable capacitor which determines the frequency of the LPF and the frequencies of the respective circuits are determined as 160 fH, 4.21 MHz and 1.3 MHz.

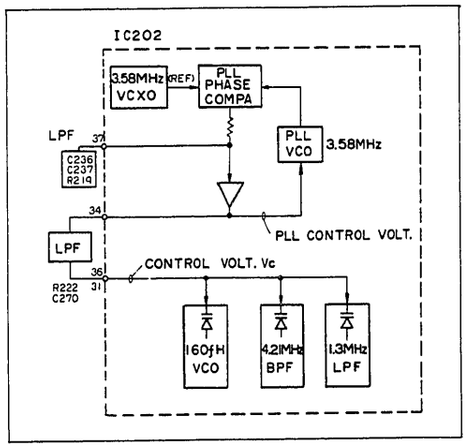


Fig. 4-43 Filter Principle Diagram (Chrominance)

(6) CHROMINANCE PLAYBACK PROCESS (Fig. 4-44a)

1) General

The chroma signal during playback is processed in IC202, the same as in recording. The "PB5V" signal goes "Hi" during play and this sets IC202 pin 18 to "Hi", so all switches in IC202 are changed over to the "PLAY" positions and the playback signal is routed as follows.

2) 1.3 MHz LPF Circuit

The chroma signal during playback is derived from the channel switch circuit output at IC1 pin 6 and fed to the 1.3 MHz LPF circuit.

The 1.3 MHz LPF circuit selects the chroma signal (629 kHz ± 500 kHz) mixed in the luminance FM signal and let it pass.

L297 and C290 connected to pin 28 form a trap tuned to approx. 1.5 MHz. This trap prevents the sideband of the luminance signal from entering the chroma frequency band.

L215 and C241 connected to IC202 pin 28 compose a 70 kHz audio bias trap. This eliminates the audio bias induced in the video heads in the audio dub mode. (This block is not provided in VT-1100A/1105A.)

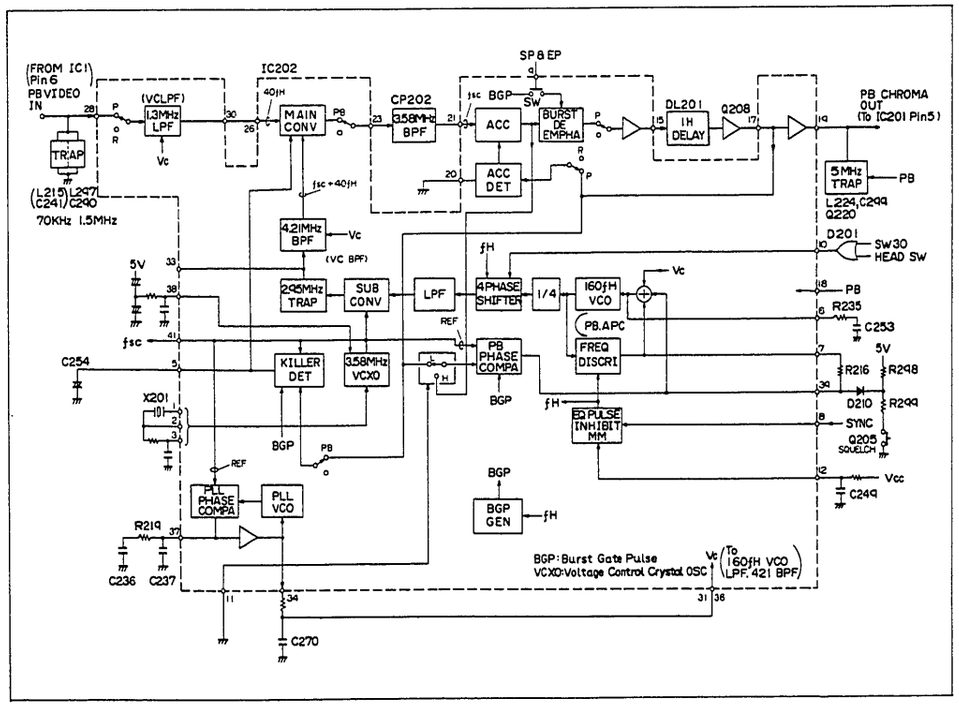


Fig. 4-44a Simplified Chrominance Playback Circuit

3) Playback Main Converter Circuit

Playback main converter converts the 629 kHz rotational unstable chroma signal from the tape to a 3.58 MHz non-rotational stable signal.

As it was explained in the general section, the two inputs to the modulator are the 629 kHz signal and a 4.21 MHz signal which has the same instability and rotation as the 629 kHz signal.

It is important that the rotation of the 4.21 MHz signal is the same direction as the 629 kHz playback chroma signal.

To obtain the 3.58 MHz non-rotational stable signal, the same direction rotational signal is mixed with the rotational chroma signal.

For this reason, after frequency conversion with the playback main converter, the subtracted signal is selected by the 4.21 MHz bandpass filter. Subtraction is performed between the 4.21 MHz and 629 kHz signals in terms of phase and frequency, so the rotation and delta factor which causes frequency fluctuations in the playback chroma signal are cancelled.

The output of the playback main converter circuit is applied to the 3.58 MHz bandpass filter circuit (CP202) via IC202 pin 23.

4) 3.58 MHz Bandpass Filter Circuit (CP202)

The 3.58 MHz BPF circuit (CP202) selects the difference component which is the chroma signal (3.58 MHz ± 500 kHz) from the output signal ((629 kHz ± 500 kHz ±Δ) ± (3.58 MHz + 629 kHz ±Δ)) of the playback main converter in the previous stage and lets it pass.

The output of the 3.58 MHz BPF circuit is applied to the ACC circuit via IC202 pin 21.

5) ACC Circuit

The role and basic operation of the ACC circuit are the same as in the record mode. The output of the ACC circuit is applied to the Burst Deemphasis circuit.

6) Burst Deemphasis Circuit

The chroma burst signal is emphasized by 6 dB in the SP and EP modes (not in the LP mode) during recording, so the burst deemphasis circuit halves the playback burst amplitude to demodulate the original amplitude.
In the SP and EP modes being applied with a high potential via pin 9, the switch turns "on" and applies the burst gate pulse to the burst deemphasis circuit. With the burst gate pulse given, the burst deemphasis circuit reduces the burst amplitude to half. In the LP mode the burst deemphasis circuit operates as an ordinary amplifier because pin 9 is "Lo", the switch is "off" and burst gate pulse is not applied to the burst deemphasis circuit.

The output of the burst deemphasis circuit is applied to the 1H Delay circuit via IC202 pin 15.

7) 1H Delay Line Filter circuit (Fig. 4-44)

In order to greatly reduce the chroma crosstalk which can occur during playback (especially in LP and EP modes), a 1H delay line filter is used.

The purpose of the 1H delay line filter is to add together the delayed and undelayed chroma signals, which doubles the desired chroma signal and eliminates the crosstalk.

The output of the 1H delay line filter circuit is applied to the Buffer amplifier circuit via IC202 pin 17 and to ACC detector circuit and color killer detector circuit.

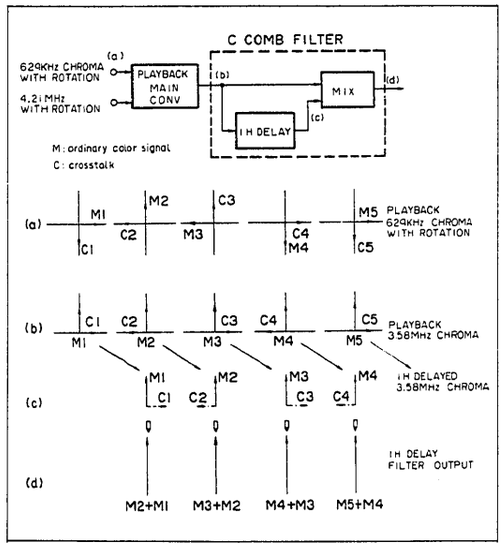


Fig. 4-44 Color Crosstalk Cancellation

8) 3.58 MHz VCXO

The oscillation frequency of this 3.58 MHz VCXO is synchronized with the burst signal in the video signal during recording. During playback, the 3.58 MHz VCXO generates a signal with a frequency determined by the crystal oscillator connected to pins 1 and 2, in the free-run mode.
The frequency of the chroma burst signal during playback is aligned with the oscillation frequency of this 3.58 MHz VCXO.

Frequency fluctuations of the chroma burst signal caused by jitter, etc. during playback are detected using the output frequency of the 3.58 MHz generator and removed in PB main converter.

9) 40 fH Generator

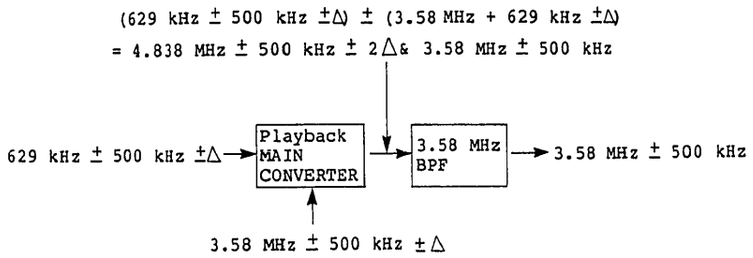
The role and basic operation of the 40 fH GEN are similar to those in recording, but the 160 fH VCO phase control loop differs from that in recording.

(a) 160 fH VCO control loop

The comparator output, obtained by comparing the 3.58 MHz VCXO phase with the chroma burst signal supplied from the 1H delay line circuit, is applied to the 160 fH VCO circuit. The 160 fH VCO oscillates to produce a frequency which contains same frequency fluctuations as those in the burst signal (±Δ), and supplies it to the playback main converter via 1/4 divider, 4-phase shifter, 4.21 MHz sub

converter, 4.21 MHz BPF and cancels frequency fluctuations

(±Δ) of the chroma signal caused by jitter, etc.


(629 kHz ± 500 kHz ±Δ) ± (3.58 MHz + 629 kHz ±Δ)
= 4.838 MHz ± 500 kHz ± 2Δ& 3.58 MHz ± 500 kHz
629 kHz ± 500 kHz ±Δ
Playback MAIN CONVERTER
3.58 MHz BPF
3.58 MHz ± 500 kHz
3.58 MHz ± 500 kHz ±Δ

(b) Frequency discriminator

The 160 fH VCO is controlled by the frequency discriminator as well as the PB APC phase comparator output in the play mode to remove the PB 3.58 MHz chroma frequency fluctuation. The 160 fH VCO has a wide variation range. The frequency may be drifted greatly from 2.52 MHz during transients such as when power is supplied. The frequency discriminator operates to set the frequency of the 160 fH VCO correctly to 2.52 MHz at this time. The frequency discriminator outputs until it is locked to the correct frequency (160 fH). The frequency discrimination is performed digitally for precision. When the 160 fH VCO oscillates at 160 fH correctly, the number of pulses output from the VCO in the 1H period is set to exactly 160. For example, when it oscillates at 164 fH, the number of the pulses is 164 increasing by 4. The oscillation frequency can be found correctly by counting the number of the pulses of the VCO for 1H period. The 1H period is the repetition period of the horizontal sync pulse itself, so it can be set very precisely.

Actually, the frequency discriminator discriminates the frequency variation when the frequency has deviated by more than +1/2 fH. The pulse count is done for the 4H period to discriminate the +1/2 fH deviation. For that purpose, the frequency discriminator output is applied to the 160 fH VCO to increase the frequency of the 160 fH VCO when the number of the pulses in the 4H period is 638 or less and to decrease the frequency of the 160 fH VCO when the number of pulses is 642 or more (160 x 4 = 640). The frequency discriminator is not shown in the schematic diagram because the schematic becomes complicated.

4-2-5 RF Converter/Output Selector

Fig. 4-10(h) is a simplified diagram of the RF converter /output selector circuits. These circuits are housed in one shielded case. The RF converter IC1 becomes active when the VTR5V B+ (produced by the TV/$\overline{\text{VTR}}$ mode setting output at pin 12 of T-μP and switch Q503: Not shown) is applied to the B+ input at pin 8 and generates the picture-RF signals (fp), AM-RF converts the video signal and FM-RF converts the audio signal. The fp signal has two frequencies aligned with channels 3 and 4 (61.25 MHz: Channel 3, 67.25 MHz: Channel 4), one of the frequencies can be selected by the operator. The fp signal is generated by the dual resonator (SAW) resonating with frequencies 61.25 MHz and 67.25 MHz and the fp oscillator in the IC. The 61.25 MHz resonator output of the SAW is applied to IC1 pin 9 and the 67.25 MHz resonator output is applied to pin 10. One of fp signals is selected by the RF channel setting voltage at pin 7 of IC1. The voltage at pin 7 is the RF channel switch input. When channel 3 is selected, pin 7 goes "Hi" and the resonant frequency at pin 9 is selected, and when channel 4 is selected, pin 7 goes "Lo" and the frequency at pin 10 is selected, then the selected frequency signal is connected to the fp oscillator.

The fp oscillator generates the fp signal corresponding to the selected channel and applies the output to the video amplitude modulator and FM audio RF mixer. The video signal from the video processing

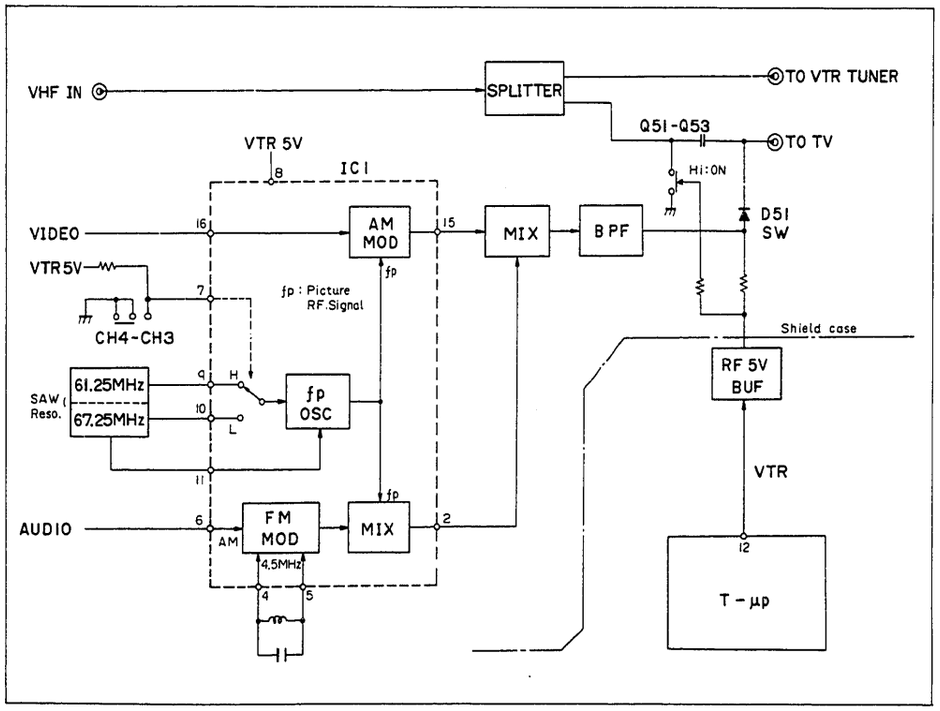


Fig. 4-10(h) Simplified RF Converter/Output Selector Circuit Diagram

circuit is supplied to the video amplitude modulator in IC1 via the video input at pin 16 and modulates the fp signal. The AM-RF converted video signal is output at pin 15 and is supplied to the video/audio mixer.
The audio signal from the audio processing circuit is supplied to the 4.5 MHz frequency modulator in IC1 via pin 6. The 4.5 MHz frequency modulator generates an audio signal with its frequency modulated in proportion to the amplitude of the audio signal centering the resonant frequency of the 4.5 MHz resonator circuit connected to pins 4 and 5, and applies the output to the audio RF mixer. The audio RF mixer mixes the previously described picture RF carrier signal and 4.5 MHz FM audio signal and outputs the resultant signal at pin 2. The FM-RF audio signal at pin 2 is supplied to the video/audio RF mixer. The video/audio RF mixer mixes the AM-RF video signal and FM-RF audio signal. The mixed channel 3 or 4 RF signal component is passed through the bandpass filter (BPF), set to the frequency of the channel 3 or 4 signal component, and switching diode D51 and is supplied to the VHF RF output. The VHF RF output also receives the antenna RF signal input from the VHF antenna input terminal. When the VTR/TV switch is set to "VTR", since the switching transistors and diode Q51 - Q53 and D51 are turned "on" by the VTR5V B+, the antenna RF signal is grounded via Q51 - Q53 and the RF signal from the RF converter is supplied to the VHF RF output via D51. When the VTR/TV switch is set to "TV" mode, since D51 and Q51 - Q53 turn "off", the antenna RF signal is supplied to the VHF RF output and the RF signal from the RF converter is interrupted by D51. The output at the VHF RF output terminal is applied to the monitor TV.

5. MECHANISM DESCRIPTION

1. Overview

The basic operations and locations of components of the chassis used in "1000" series VTRs are the same as in X chassis in "60" series VTRs. The following items have been changed and improved.

1-1. The reel drive system has been changed to the gear drive from rubber tyre drive.

1-2. A guide pin has been added to the take-up side. (behind the capstan)

1-3. The front loading mechanism in this chassis is the same as that in the X chassis.

1-4. The capstan bearing is retained by three (3) screws not by caulking.

2. Operations of Each Section

2-1. Components Locations (Fig. 5-1)

The tension band is provided for the supply reel table to control the tension in supplying the tape and the supply sub-brake is installed to apply weak back torque to the supply reel disk during fast forward and rewind.

The impedance roller is next to the full erase (FE) head and absorbs variations in tension of the tape to reduce jitter.
The cylinder is the same type as in conventional VTRs, but a connection P.C.B is provided in the cylinder to prevent noise from entering the upper cylinder from outside.
The lead wires of the heads are not soldered but connectors are used.

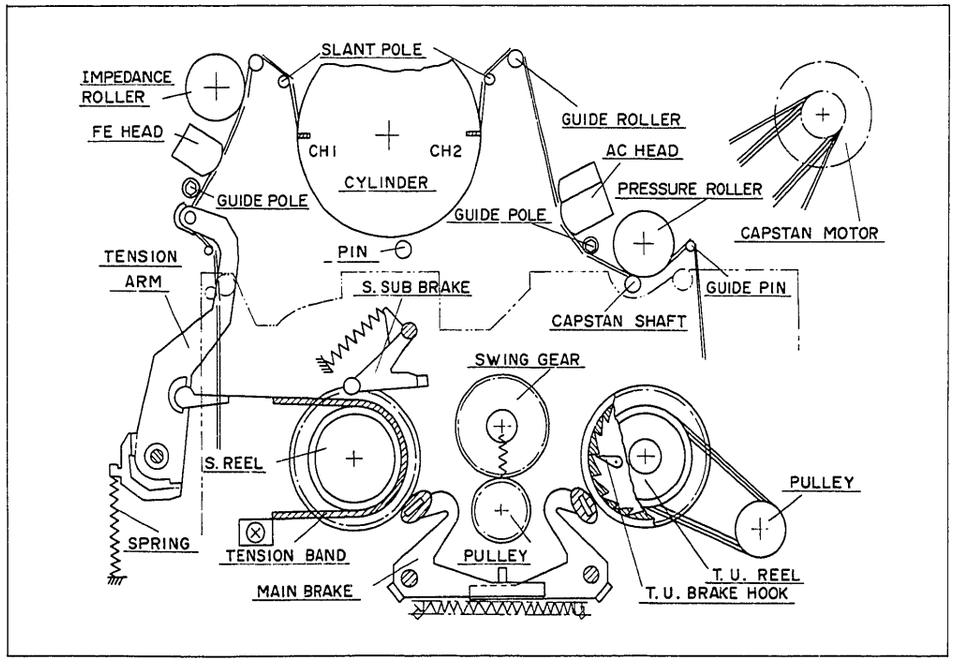


Fig. 5-1 Parts Arrangement

This simplifies replacement of the upper cylinder.
The A/C head consists of the audio head, control head and audio erase head as in conventional VTRs.
The tape guide is installed next to the A/C head and controls the height of the running tape.
The capstan and pressure roller have the same structures as conventional ones, but the flywheel bearing is tightened by three (3) screws, not by caulking.
The guide pin is provided beside the capstan to stabilize the tape transport.
The take-up brake hook is inside the take-up reel table to apply weak back torque in the search modes.
The pulley gear is in the middle of both reel tables, and torque is transmitted to this gear from the capstan motor to drive both reel tables via the swing gear.
Teeth are provided on the external circumference of this swing gear, and to mesh with these, both the reel tables have teeth in their circumferences.
The main brakes operate the same as before.

2-2. Loading Mode (Fig. 5-2)

When the loading motor at the left corner in the chassis turns clockwise, loading is performed.
When the PLAY button is pressed in the stop mode, first the loading motor turns in the loading direction (clockwise as viewed from the shaft axis) and the main brakes are released from both reel tables by the main brake drive mechanism (see Fig. 5-7). When the loading motor turns further, both guide roller assemblies move along the guide grooves in the chassis. When the guide roller assemblies approximately reach the arm stoppers, the mechanism state switch detects the 4th contact "PLAY" and stops turning the loading motor.

During loading, by the operation of the loading drive arm engaged with gear (R) and gear (L) (shown in Fig. 5-7), braking is applied to the supply reel table by the supply sub brake to prevent tape slack when the tape is supplied. Braking is applied to the take-up reel table by the take-up brake hook in this reel table during loading.
Just before loading is completed, the supply sub-brake is released from the supply reel table and the take-up brake hook is released from the gear in the take-up reel table by the operation of the loading gear assembly. The pressure roller is compressed against the capstan shaft and the mechanism enters the playback mode. The tension band is moved by the spring force as the supply guide roller assembly advances, and as soon as the playback mode is entered, it operates to control the supply tape tension.

2-3. Unloading Mode (Fig. 5-3)

When the STOP button is pressed in the playback or record mode, the loading motor turns counterclockwise (as viewed from the shaft), and the guide roller assemblies, installed to the link arm which is engaged with gears (L) and (R) (shown in Fig. 5-7), move along the grooves in the chassis and return to the stop positions.

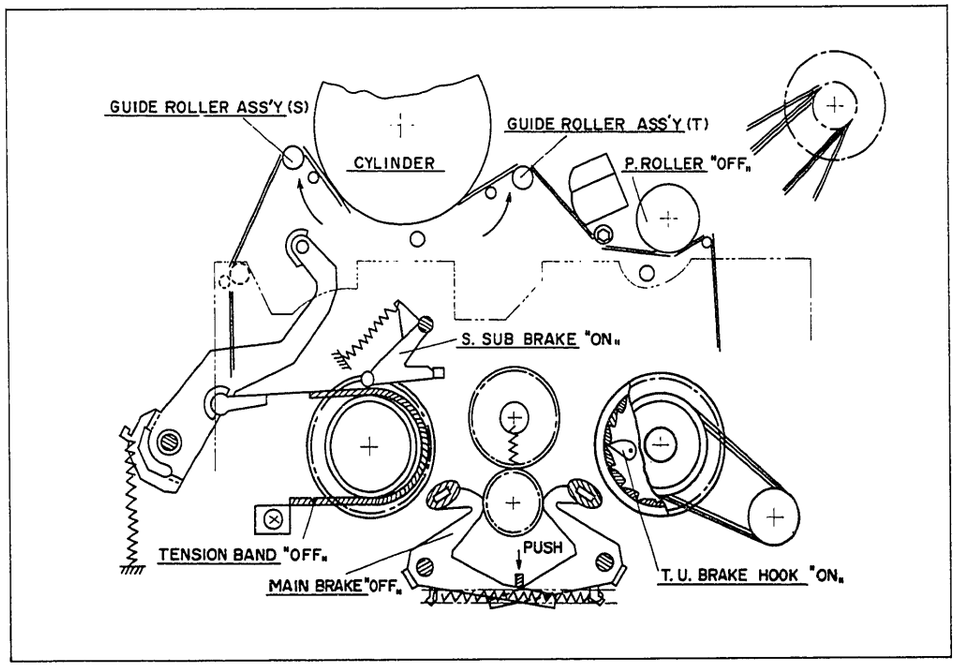


Fig. 5-2 Loading Mode

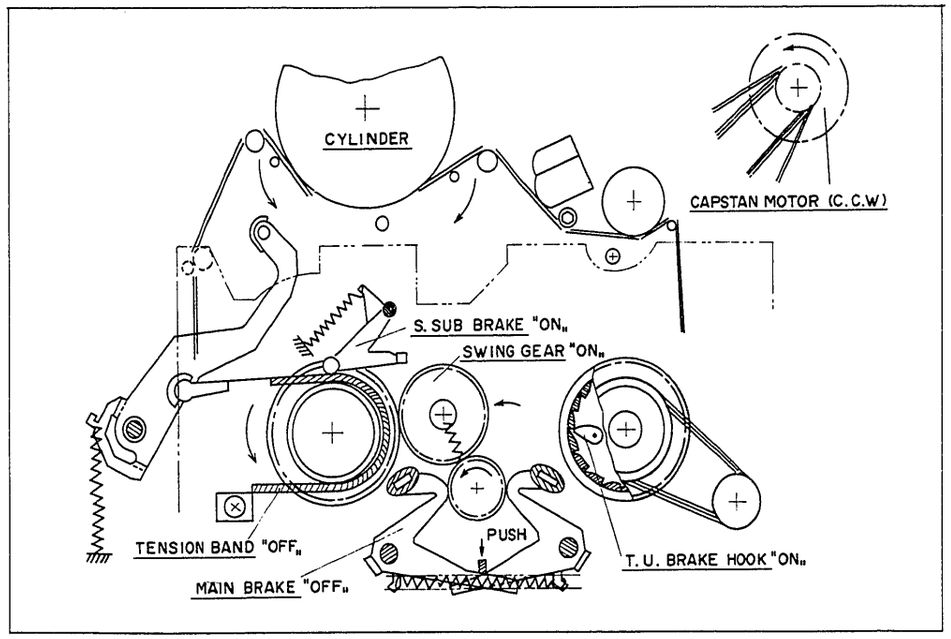


Fig. 5-3 Unloading Mode

To take up the tape supplied, the capstan motor turns counterclockwise. This series of the operations compresses the swing gear against the supply reel table and turns the supply reel table counterclockwise to house the tape in the cassette case.
During unloading, the supply sub-brake is compressed against the supply reel table and the take-up brake hook is engaged with the gear in the take-up reel table during loading.

2-4. Fast Forward Mode (Fig. 5-4)

When the F.FWD button is pressed in the stop mode, the loading motor turns clockwise and releases the main brakes from both reel tables. As the capstan motor turns clockwise, the swing gear is compressed against the take-up reel table and turns the reel table at high speed to take up the tape. Meantime, the supply sub-brake is compressed against the supply reel table to prevent the tape becoming slack during fast forward. The take-up brake hook and the gear in the take-up reel are disengaged each other.

2-5. Rewind Mode (Fig. 5-4)

The mechanism state is almost the same as during fast forward, but the capstan motor rotates counterclockwise at high-speed. Weak back torque is applied to the take-up reel table because the pulley rotates to prevent the tape becoming slack.

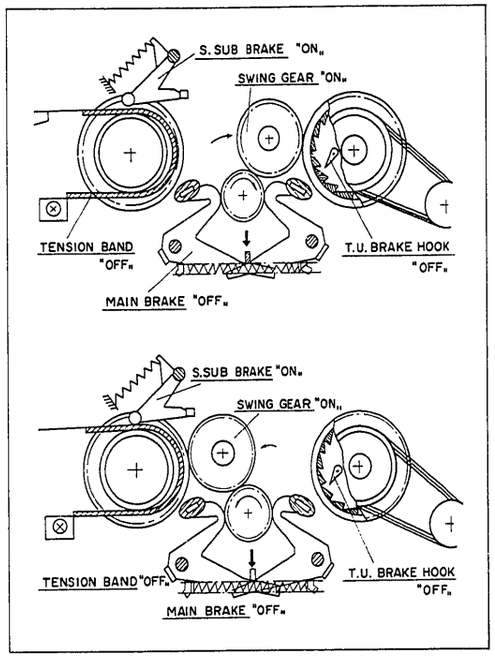


Fig. 5-4 F.Fwd/Rewind Modes

2-6. Reel Drive Path in Play and unloading Modes (Fig. 5-5).

Both the supply and take-up reel tables must be driven at the appropriate torque in the play and unloading modes. This is because the torque transmitted from the capstan motor is limited by the slip mechanism provided on the take-up pulley and is then transmitted to both reel tables. The torque transmitted to the belt pulley in Fig. 5-5 is transmitted to the take-up pulley via the belt.

The slip mechanism provided in the upper part of the take-up pulley limits the torque from the capstan motor to an appropriate value and it is transmitted to the pulley gear via the take-up gear, idler gear, and clutch gear. The swing gear compressed against the pulley gear swings its neck to the left and right and is compressed against both reel tables to transmit the torque. Meantime, the clutch gear is pushed up by the clutch lever and is engaged with the idler gear. This operation is performed by the drive arm engaged with the gear (R) as the loading motor rotates.

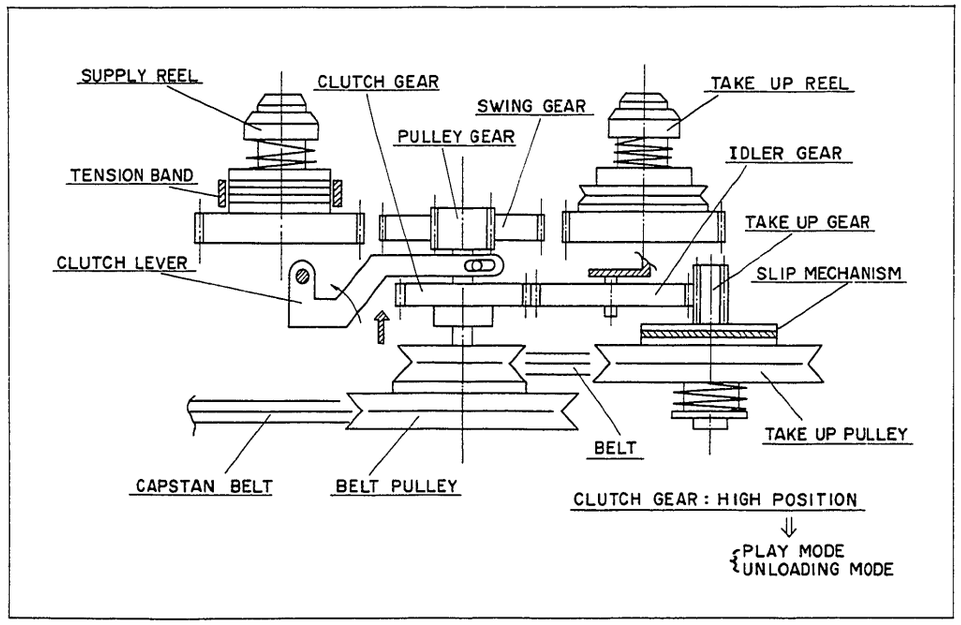


Fig. 5-5 Reel Drive in Play/Unloading Modes

2-7. Reel Drive Path in F.Fwd and Rewind Modes (Fig. 5-6)

Since strong torque must be applied to both reel tables in the fast forward and rewind modes, the torque from the capstan motor should not be limited and transmitted directly to both reel tables. When the F.FWD or REWIND button is pressed in the stop mode, the loading motor turns clockwise and the mechanism state switch detects the 2nd position, then the turning of loading motor is stopped. During these operations, simultaneously when the main brakes are released from both reel tables, the clutch gear is pushed down and the engagement with the idler gear is released. When the clutch gear is depressed, it engages with the belt pulley directly, and the torque from the capstan motor is transmitted directly to the pulley gear without any slipping.
The weak torque which is transmitted via the slip mechanism is not transmitted to the pulley gear because the idler gear and clutch gear are disengaged each other.

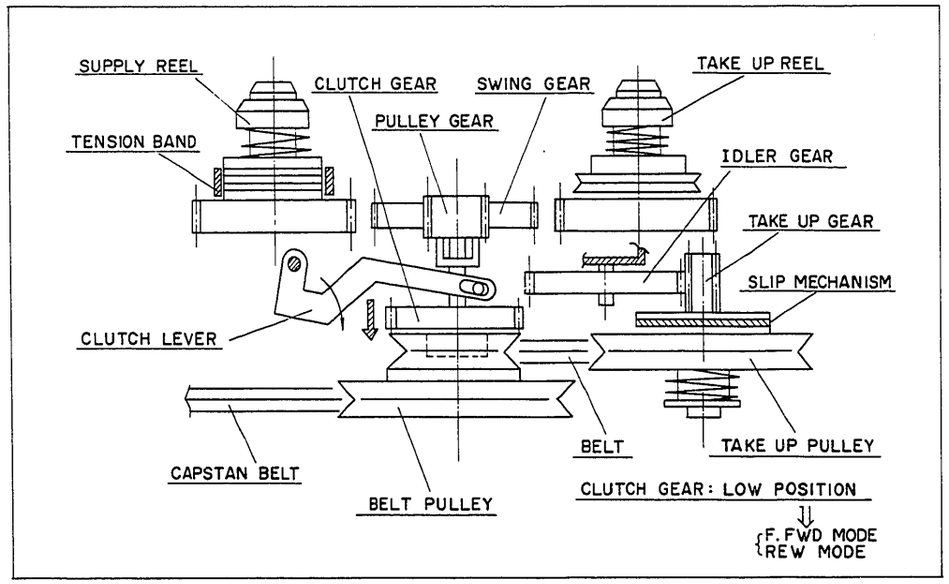


Fig. 5-6 Driving Path (F.Fwd/Rewind Modes)

2-8. Main Brake Drive Mechanism (Fig. 5-7)

When the PLAY, F.FWD or REWIND button is pressed in the stop mode, the loading motor turns clockwise and drives the worm gear via three (3) pulleys. This worm gear is engaged with the gear (R). The guide groove is provided on the gear (R), and the drive arm engaged with this groove pulls the brake slider to the left in Fig. 5-7 as the loading motor turns. The projection on the slider is engaged with the recess in the lock plate, and when the slider moves to the left, the brake slider is also pulled to the left. Through this operation, the ramp X (See Fig. 5-7) of the brake slider depresses the main brake drive pin in contact with this ramp downward in Fig. 5-7. When the main brake drive pin is pressed in the direction of the arrow in Fig. 5-7, the main brakes are released from both reel tables and braking is released.
When the lock plate passes under the change piece and touches it, the rotation of the change piece slips and the engagement between the lock plate and slider is not released and the lock plate moves to the left and is set to the position shown in Fig. 5-7 (a).

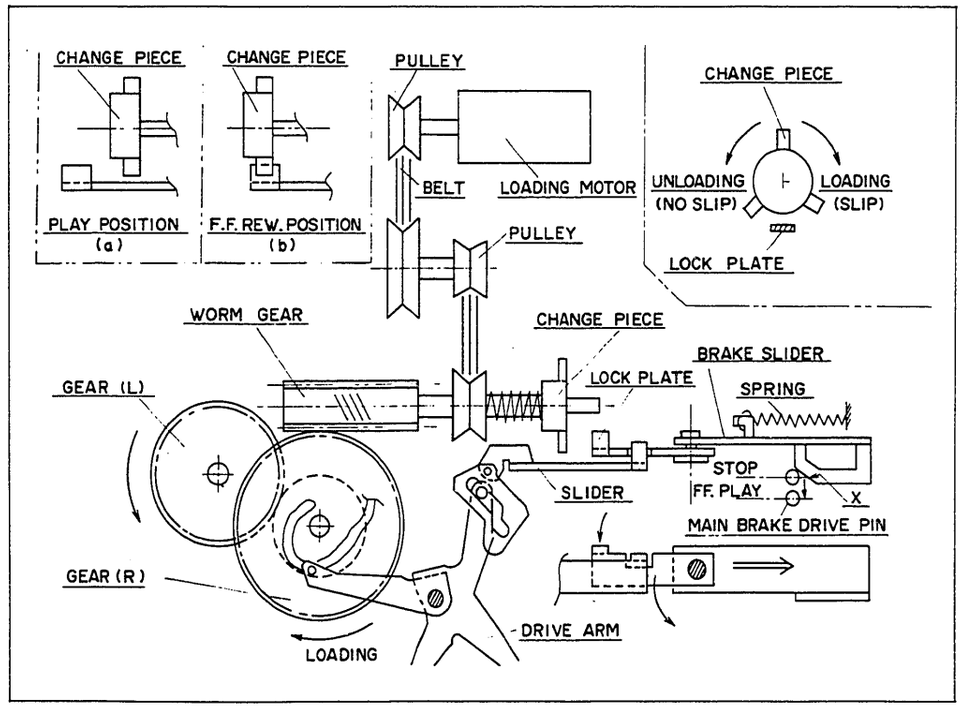


Fig. 5-7 Main Brake Drive Mechanism

piece, the mechanism state switch detects the 2nd position and stops turning the loading motor. That is, the lock plate is set to the position in Fig. 5-7 (b).
When the main brakes are applied, for example when the STOP button is pressed in the playback mode, the lock plate moves to the right from the state shown in Fig. 5-7 (a). When the lock plate reaches under the change piece, it is pushed down by the projection on the change piece. With this operation, the engagement between the slider and lock plate is released and the brake slider is rapidly moved to the right by the spring force. Since the main brake drive pin which is in contact with the ramp of the brake slider is compressed against this ramp, accompanying with the rapid shift of the brake slider, the pin is rapidly pushed up as shown in the figure and the main brake operates.
When the main brakes is applied in the fast forward mode, since the lock plate is set under the change piece as shown in Fig. 5-7 (b), simultaneously when the stop button is pressed and the loading motor starts turning counterclockwise, the change piece also turns counterclockwise. With this operation, as the change piece pushes down the lock plate, the engagement between the slider and lock plate is released, and the main brake is applied.
When the projection on the change piece comes into contact with the lock plate during loading, the turning of the change piece slips and it does not depresses the lock plate. During unloading, the turning of the change piece does not slip and the change piece pushes down the lock plate.

2-9. Operation Chart (Fig. 5-8)

This chart shows the operation timing of the main components. "ON" means that the component is operating and "OFF" means that the component is not operating or is being released. As can be seen in the chart, the take-up brake hook in the take-up reel table operates in the reverse search mode as well as during loading and unloading.

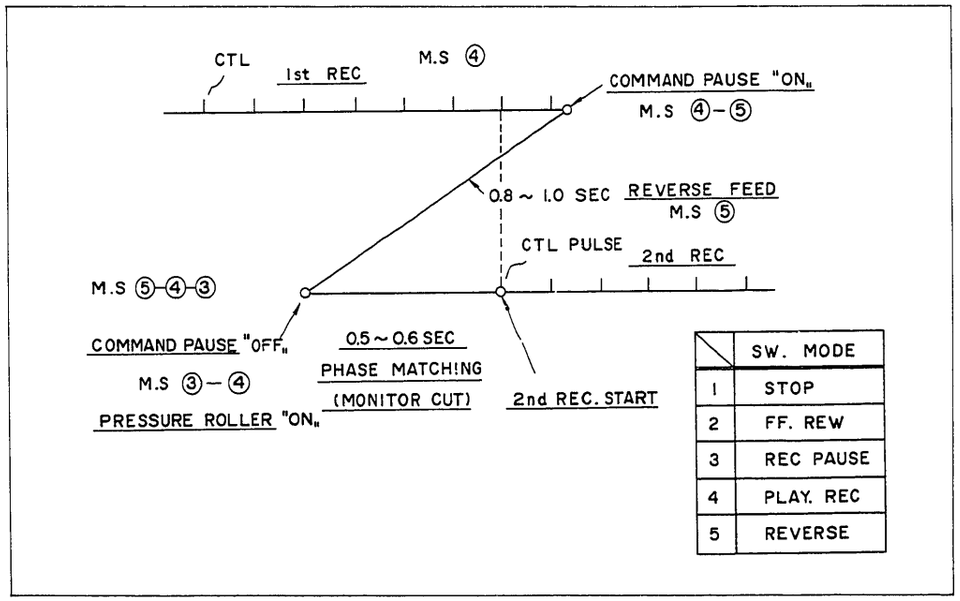
	MODE SWITCH POSITION	OPERATION MODE	S.SUB BRAKE	T.U. BRAKE HOOK	PRESSURE ROLLER	TENSION BAND	REMARKS
1	STOP	STOP	ON	ON	OFF	OFF	
							MAIN BRAKE IS RELEASED
2	FF REW	F. FWD, REWIND	ON	OFF	OFF	OFF	
3	REC-PAUSE	REC PAUSE	ON	ON	OFF	OFF	
4	REC/PLAY	REC, PLAY, PLAY-PAUSE, FORWARD VISUAL SEARCH	OFF	OFF	ON	ON	
5	REVERSE	REVERSE VISUAL SEARCH	OFF	ON	ON	OFF	

Fig. 5-8 Operation Chart

2-10. Record Pause Mode (Fig. 5-9)

In this mode the mechanism operates so the joint of pictures recorded previously and to be recorded later does not appear as distortion during playback.
When the PAUSE button is pressed in the previously record mode, the loading motor turns in the loading direction and the mechanism state switch advances to the 5th position. With this operation, braking is applied to the take-up reel table by the take-up brake hook in the take-up reel to prevent tape slack occurring when the tape is run in reverse (to the supply reel). When the capstan motor turns counterclockwise afterwards, the tape is returned to the supply reel and is stopped after approx. 0.8 seconds. After the tape is stopped, the loading motor turns in the unloading direction and the mechanism state switch is returned to the 3rd from 5th position. This operation releases the pressure roller from the capstan shaft. Then, the capstan motor changes its turninng direction to clockwise to prepare for the next start and stands by in this state (record pause mode).

When the pause mode is released, the loading motor turns in the loading direction to advance the mechanism state switch to the 4th from 3rd position. This operation compresses the pressure roller against the capstan and the tape is fed to the direction of the take-up reel.
The servo circuit performs phase matching during these operations, and after the tape speed of the tape to be played back is aligned with that during recording, the video circuit is switched to the record mode. With this operation, since the timings of the CTL pulses recorded previously and to be recorded later are aligned, the picture at the joint is not distorted during playback. This is called the phase matching mode (record pause mode).



	SW. MODE
1	STOP
2	FF. REW
3	REC PAUSE
4	PLAY. REC
5	REVERSE

Fig. 5-9 Record Pause Mode

6.1 GENERAL

Table 1-1a,b shows the differences between the VT-1310A/1305A and VT-1100A/1105A. The composition of the VT-1310A/1305A is described as follows.

Luminance/Chroma Circuit:
The "HQ" system employs new ICs revised from those in the VT-1100A/1105A for requirements of productivity and also newly employs the Detail Enhancer circuit as a exclusive IC HA11888.

System Control Circuit:
System control circuit employs the new μP revised from VT-1100A/1105A for requirements of productivity.

Tuning Control Circuit:
107CH; Voltage Synthesizer tuning control circuit employs the new μP and REG/BAND SELECTOR IC, revised from VT-1100A/1105A for requirements of productivity.

Timer Control Circuit:
4-Event/2-Week Timer control circuit employs the new μP revised from VT-1100A/1105A for requirements of productivity.

Audio Circuit:
New audio processing IC is used. The circuit configuration of the VT-1310A/1305A is very similar to that in the VT-1100A/1105A.

Servo Circuit:
Same as in VT-1100A/1105A except that;
Time constant components for each MMs in the main servo processing ICHA11853, low-pass filters and limiters on the SERVO SUB board in the VT-1100A/1105A are integrated into two modules, BX6238 and BX6239.

Miscellaneous Circuit:
Other circuits are almost the same as VT-1100A/1105A .

Table 6-1a (Y)/(PY) Chassis Comparison Table

#	ITEM	Y	PY	NOTE
1	MECHANISM	Y MECHA	SAME AS Y	
2	LAYOUT		SEE ACTUAL UNIT	
3	P.C.B	A) LUMINANCE/CHROMINANCE B) AUDIO JACK SYSTEM CONTROL SERVO CAPSTAN DRIVER U-V TUNER U-V TUNING C) REGULATOR CYLINDER DRIVER D) TIMER AND KEY	A) LUMINANCE/CHROMINANCE AUDIO JACK U-V TUNER U-V TUNING B) SYSTEM CONTROL SERVO CAPSTAN DRIVER CYLINDER DRIVER C) REGULATOR D) TIMER AND KEY	
4	CIRCUIT COMPONENT ("HT-" and "BX-" means hybrid IC)	HT-4705 HT-4723 HT-4495 HT-4497	HT-4765C HT-4763 HA-11888 M51485L MSM6964	LUMINANCE
		HA11856	HT4706	CHROMINANCE
		BA5119S	M51654AP	AUDIO
		HA11853 TRANSISTORS	HA11853 HA11887	SERVO
		SERVO SUB (I) (II) CIRCUIT BOARD	BX-6238 BX-6239 (3 heads) BX-6240 (2 heads)	
		SYSTEM CONTROL MICROPROCESSOR	REFINED TO INTEGRATE SOME COMPONENTS	SYSTEM CONTROL
		LA7934	LA79356	TUNING CIRCUIT
		TUNING MICROPROCESSOR	REFINED TO INTEGRATE SOME COMPONENTS	
		TIMER/INPUT KEY/FUNCTION SW	SAME AS Y	
		TIMER MICROPROCESSOR	SAME AS Y	
		STK-5471	STK-5471	REGULATOR
		TUNER	SLIGHTLY CHANGED BY REFINING TUNING MICROPROCESSOR	
		RF CONVERTER	SAME AS Y	

Table 6-1b Difference between VT-1100A/1105A & VT-1310A/1305A (Circuit)

ITEM \ MODEL		VT-1100A/1105A	VT-1310A/1305A	NOTE
CHASSIS		Y	PY	
LUMA		HT-4755	HT-4765C	
		HT-4723	HT-4763	
		HT-4495	HA-11888	DETAIL ENHANCER
		HT-4497 (MSM6964 is mounted)	M51485L MSM6964	2fsc OSC CCD 1H DELAY LINE
CHROMA		HA11856ANT	HT-4706	
CYLINDER	SHAPE	MOUNT TYPE OF PREAMP	SAME AS Y	
	MOTOR	3-PHASE	SAME AS Y	
SERVO		HA11853	HA11853	
		SOME TRANSISTORS	HA11887	CFG AMP
		SUB P.C.B	BX-6238 BX-6239	
SYSTEM		HD614042SD76	HD614042SE43	
TUNING CIRCUIT		LA7934 M50161-452	LA7935 M50161-454	
TIMER		M50752-635	M50752-622	
TUNER				REFINING VS µCON, AUDIO MUTING
AUDIO		BA5119S	M5165AP	

6-2 LUMINANCE/CHROMA

6-2-1 Comparison of IC Functions

Differences between VT-1310A/1305A and VT-1100A/1105A in Luminance/Chroma Circuit are shown in Table 6-2.

Table 6-2 Comparison of IC Functions between VT-1310A/1305A and VT-1100A/1105A

	IC Code		Major Difference and Function
	VT-1310A/1305A	VT-1100A/1105A	
IC201	HT4765C	HT4755	∘ Detail Enhancer circuit is moved to exclusive IC (IC203). ∘ External Phase Compensation circuit (Q202/Q204/Q222) is integrated into this IC. ∘ AGC Switch in IC205 (HT4763) is integrated into this IC.
IC202	HT4706A	HA11856 ANT	∘ Peripheral circuits are integrated into this IC. ∘ Monitor Cut Switch (Q205) ∘ Output Buffer Amplifier (Q208) of Delay Line (DL201). ∘ 3.58MHz BPF (Q226) ∘ 3.58MHz Crystal Oscillator ∘ Peripheral resistors and capacitors
IC203	HA11888	--	∘ Detail Enhancer in IC201 is moved to this exclusive IC. (Works during recording mode at all tape speeds SP/LP/SP) ∘ This circuit works as a buffer amplifier during playback mode (equivalent to IC208 in VT-1100A/1105A)
IC204	MSM6964	HA4497	∘ Monolithic IC MSM6964 integrated in Hybrid IC HA4497 is employed indendently as a new circuit. ∘ Doubler circuit in HA4497 is moved to IC206.
IC205	HT4763	HT4723	∘ AGC Switch circuit is moved to IC201. ∘ PB5V Switch (Q206) is integrated into this IC.
IC206	M51485L	--	∘ Doubler circuit is moved from IC204 HA4497 ∘ LEVEL SHIFT (MUTE SW) Q216 and Q217 are integrated into this IC. ∘ Buffer Amplifier is moved from IC204. ∘ 9V Regulator circuit is incorporated and supplys 9V for IC203 and IC204.

6-2-2 Detail Enhancer Circuit Operation

As shown in Fig. 6-1, the input signal passing through the detail enhancer is applied to the adder circuit via R211, R212 and C253 and is added to the input signal directly applied to the adder, thus the enhancer characteristic is produced.

The detail enhancer circuit works during recording at all tape speeds, SP, LP and EP.

The enhancer characteristic is almost the same as that of the VT-1100A/1105A.

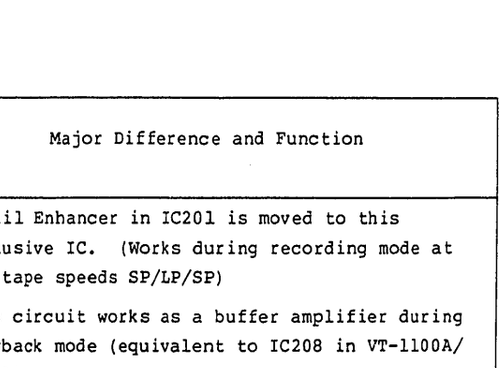


Fig. 6-1 Detail Enhancer Circuit

6-2-3 Circuit Blockdiagram

Fig. 6-2 to Fig. 6-5 are simplified Luminance/Chrominance Record/Playback Circuit Blockdiagrams.
Meshed portions are changed blocks from the VT-1100A/1105A.

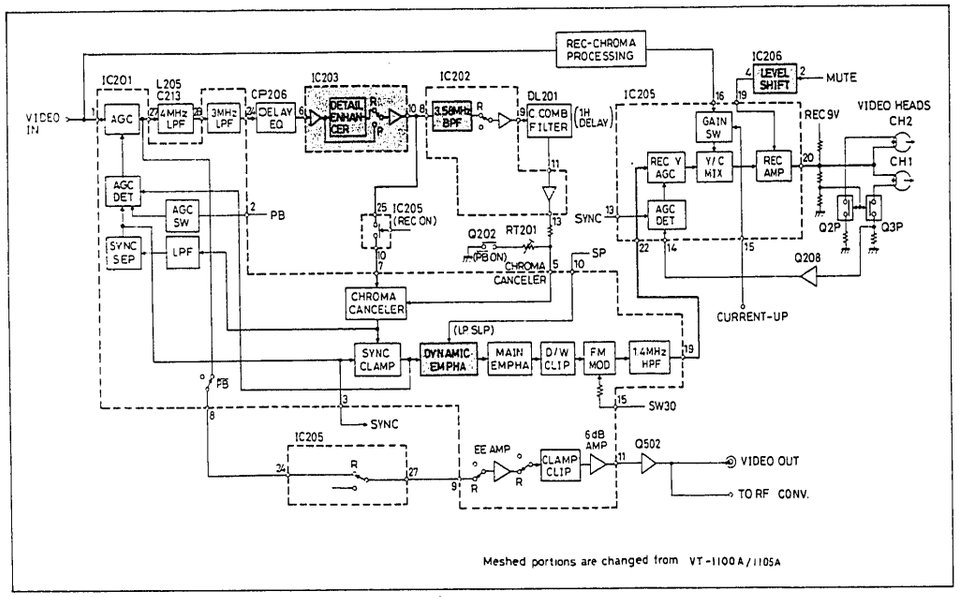


Fig. 6-2 Simplified Luminance Record Circuit Diagram

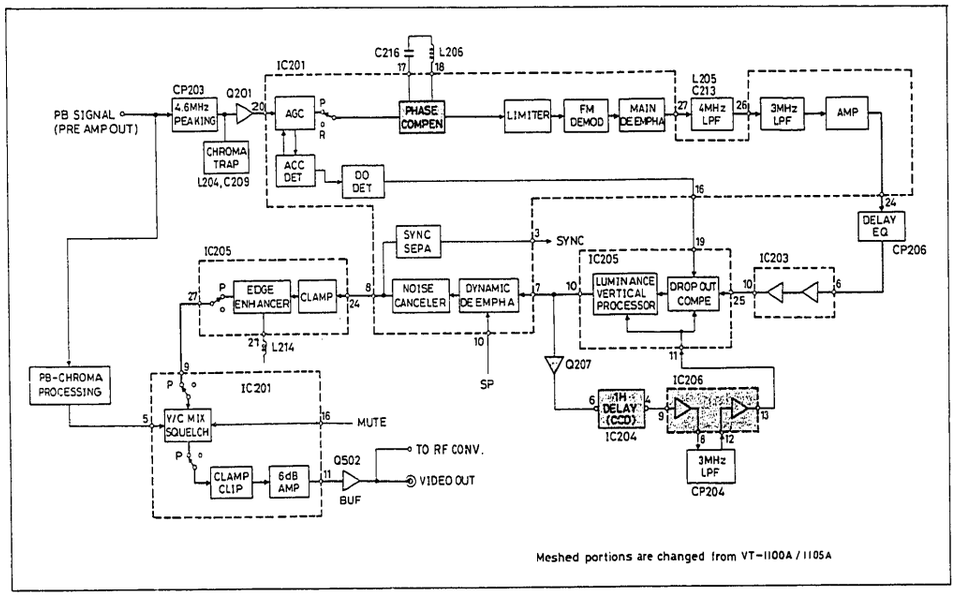


Fig. 6-3 Simplified Luminance Playback Circuit Diagram

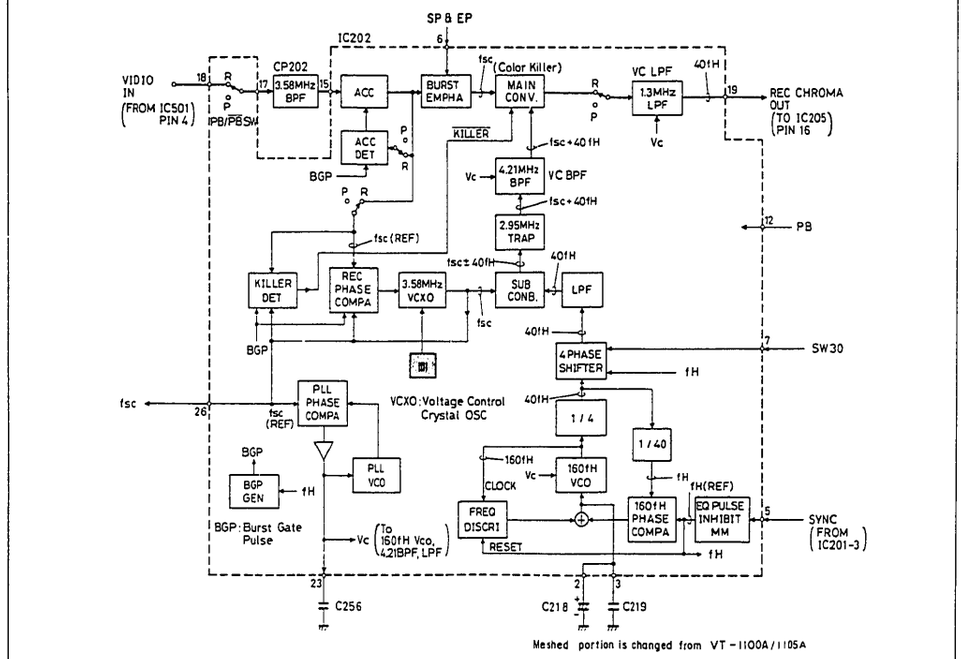


Fig. 6-4 Simplified Chrominance Record Circuit Diagram

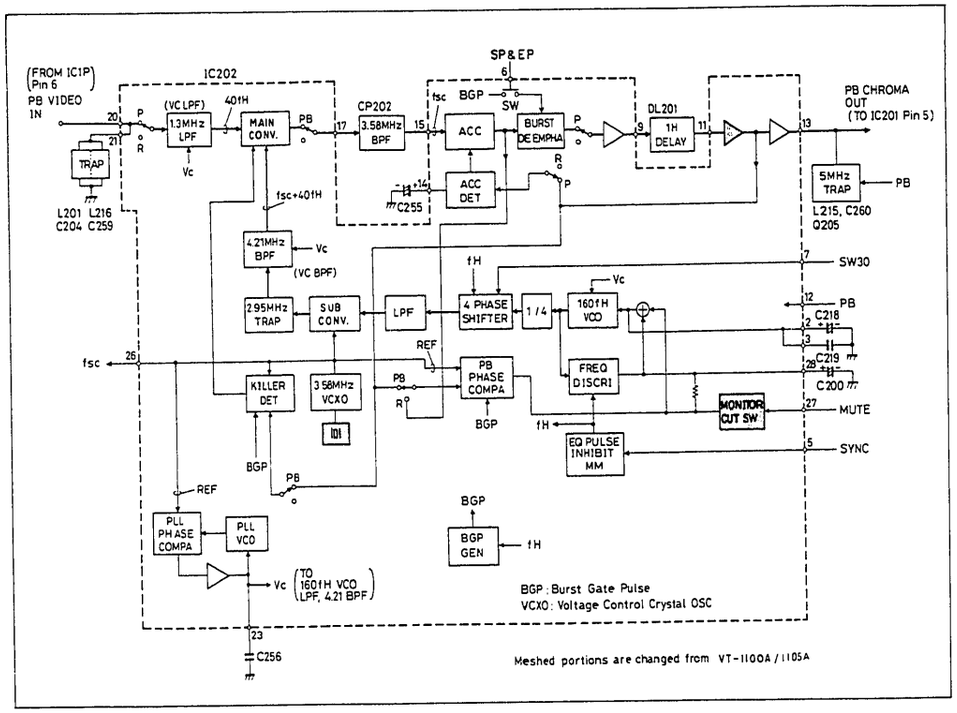


Fig. 6-5 Simplified Chrominance Playback Circuit Diagram

6-3 SYSTEM CONTROL

6-3-1 General

Fig. 6-6 is a simplified system control circuit diagram of VT-1310A/1305A. In this figure, there are only 1 differences from VT-1100A/1105A, the VTR mode indication is added to Digital multidisplay. But the following items regarding system control and tuning control μPs are revised from these in the VT-1100A/1105A.

Following items are the revised points in each μP.

S-μP:
Trick play signal, ASBL REC MUTE signal, pause/F.ADV signal and SP/LP/EP signal for the requirements of productivity.

Tu-μP:
AFC signal, Mute signal, Reset signal, 5.0V output and current source for the requirements of productivity.

T-μP:
VTR mode display and Key matrix.

6-3-2 System Control Circuit

Type of S-μP in VT-1310A/1305A and VT-1100A/1105A are HD614042SE43 and HD614042SD76 respectively. They have almost the same functions basically, except for some items shown in Table 6-3.

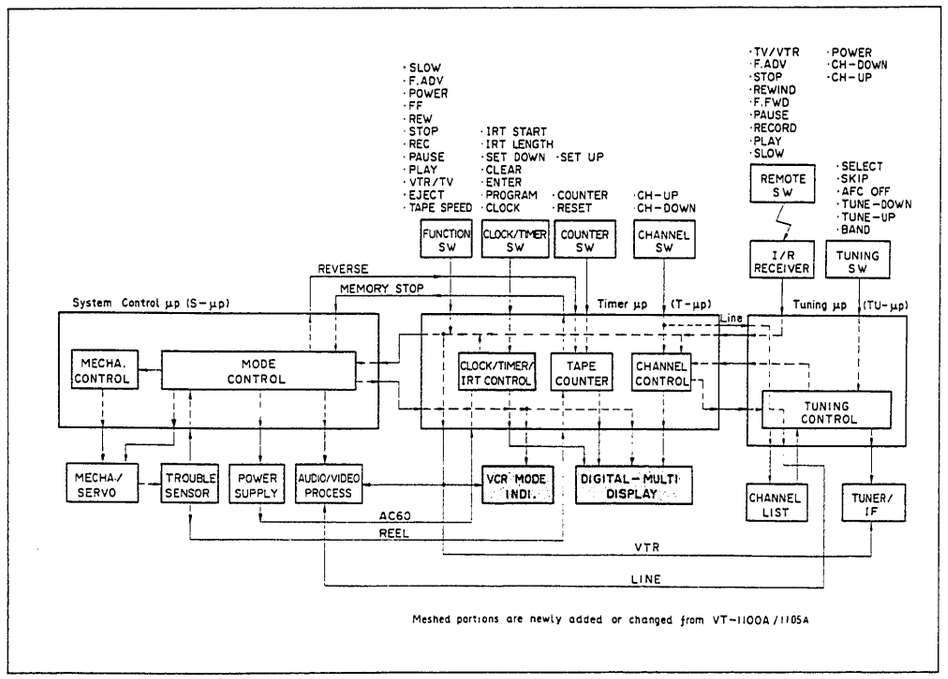
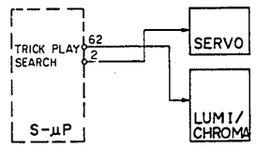
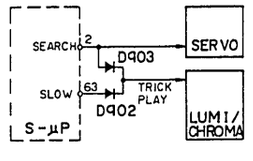
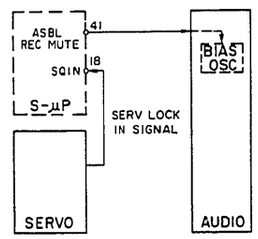
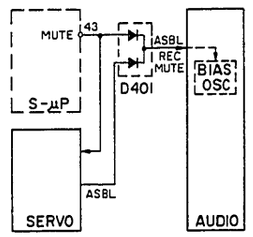
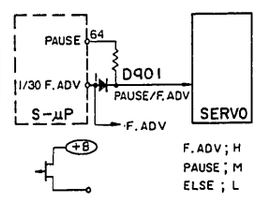
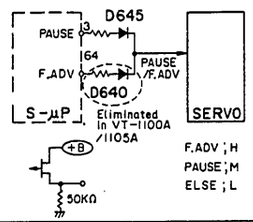
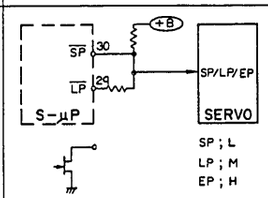
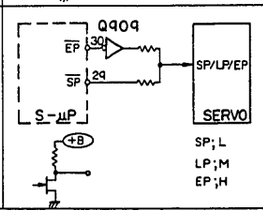


Fig. 6-6 System Control Block Diagram

Table 6-3 shows the system control circuit differences between VT-1310A/1305A and VT-1100A/1105A.

1. TRICK PLAY signal. In VT-1100A/1105A, Trickplay signal was made by adding the SEARCH signal and SLOW signal with D902 and D903. In the VT-1310A/1305A, Trickplay port (port No.62 of S-μP) is newly added and outputs High, during SEARCH and SLOW modes.
2. ASBL REC MUTE signal. In VT-1100A/1105A, ASBL REC MUTE signal was made by adding the Mute signal (S-μP port No.43) and ASSEMBLE signal from SERVO circuit with D401. In the VT-1310A/1305A, port No.18 of S-μP receives the SQUELCH signal from SERVO circuit, and port No.41 outputs ASBL REC MUTE signal (ASBL REC MUTE = MUTE + ASSEMBLE).

Table 6-3 System Control Circuit Differences between VT-1310A/1305A & VT-1100A/1105A

NO.	ITEMS	VT-1310A/1305A	VT-1100A/1105A	NOTES
1.	TRICK PLAY SIGNAL	 TRICK PLAY = SERCH + SLOW		
2.	OSC STOP SIGNAL			
3	PAUSE/F.ADV SIGNAL			Applied to VT-1310A/1305A only
4	SP/LP/EP SIGNAL			

3. PAUSE/F.ADV signal. In VT-1100A/1105A, the Tri-state signal PAUSE/F.ADV was made by adding the PAUSE signal and F.ADV signal with D640 and D645. In VT-1310A/1305A, the PAUSE/F.ADV signal is made by adding these signals without diodes. Because the output ports No.3 and 64 of the VT-1100A/1105A S-μP each have PULL-DOWN Resistors (40-160kohms) in internal circuit of the μP, but these PULL-DOWN Resistors were eliminated in VT-1310A/1305A S-μP.
4. SP/LP/EP Signal. In VT-1100A/1105A the Tri-state signal SP/LP/EP was made by adding $\overline{SP}$ signal and $\overline{EP}$ signal with inverter Q909 and resistors. Then in VT-1310A/1305A, the same signal was made by adding $\overline{SP}$ signal and $\overline{LP}$ signal with only 2 resistors. The logic and types of FETs of output ports were changed from $\overline{SP}$, $\overline{EP}$ to $\overline{SP}$, $\overline{LP}$, from N-CH output FET with PULL-UP Resistor to open Drain N-CH output FET.

6-3-3 Timer Control Circuit

T-μPs in VT-1310A/1305A and VT-1100A/1105A are M50752-622 and M50752-635 respectively. They have almost the same functions basically except some items shown in Table 6-4. Table 6-4 shows the Timer Circuit differences between VT-1310A/1305A and VT-1100A/1105A.

1. Mode display. Mode display in VT-1310A/1305A has 2-way, VTR ON, STOP and PAUSE indicator with LEDs and PLAY, REC, FF and REW indicators by Digital Multidisplay.
   On the other hand, the mode display in VT-1100A/1105A had 1-way, VTR ON, STOP, PAUSE, PLAY, REC, FF and REW indicators with LEDs.
2. Key Matrix Circuit
   Counter Reverse input port (port No.7) was added and a Matrix sw with Q753 was eliminated for the same purpose.
3. No. of Programs/Periods. Changed from 2 programs/2 weeks to 4 programs/2 weeks.

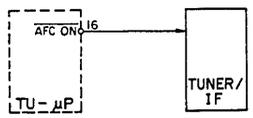
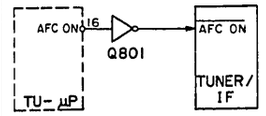
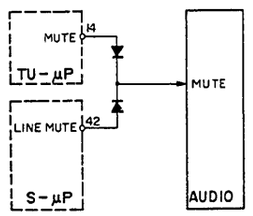
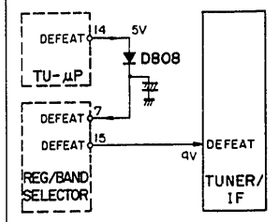
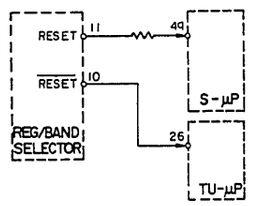
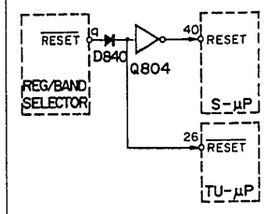
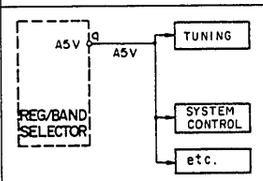
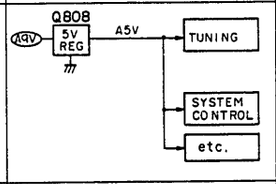
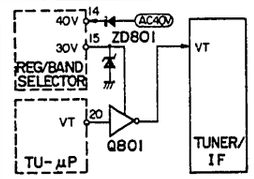
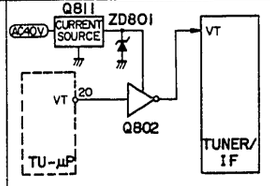
Table 6-4 Timer Circuit Differences between VT-1310A/1305A & VT-1100A/1105A

NO.	ITEMS	VT-1100A/1105A	VT-1310A/1305A	NOTES
1	MODE DISPLAY	VCR ON, STOP, PAUSE, PLAY, REC, FF, REW } BY LED INDI.	VCR ON, STOP, PAUSE } BY LED INDI. PLAY, REC, FF, REW } BY DIGITAL MULTIDISPLAY	
2	KEY MATRIX	COUNTER REVERSE Q758	(INDEPENDENT PORT NO.7)	
3	EVENT/PERIOD	2 PROGRAMS / 2 WEEKS	4 PROGRAMS / 2 WEEKS	

6-3-4 Tuning Control Circuit

Tunig μP and REG/BAND SELECTOR IC were revised from those of VT-1100A/1105A, from M50161-452SP to M50161-454SP and from LA7934 to LA7935 respectively. There is only one revised point in Tu-μP which is shown in Table 6-5 item 1. 4 points are revised in REG/BAND SELECTOR IC as shown in Table 6-5 item 2 to 5.
Table 6-5 shows the Tuning Circuit Differences between VT-1310A/1305A and VT-1100A/1105A.

Table 6-5 Tuning Circuit Differences between VT-1310A/1305A & VT-1100A/1105A

NO.	ITEMS	VT-1310A /1305A (M50161-454SP LA7935)	VT-1100A/1105A (M50161-452SP LA7934)	NOTES
1	AFC SIGNAL			
2	MUTE SIGNAL			
3	RESET SIGNAL			
4	5.0V OUT PUT			
5	CURRENT SOURCE			

1. AFC Signal. An Inverter Q801 was eliminated by changing the polarity of output port No.16 in Tu-μP from AFC ON TO AFC $\overline{\text{ON}}$.
2. Mute Signal. Audio Mute signal was supplied to Tuner/IF Mute circuit through the level shift circuit in REG/BAND SELECTOR IC to defeat tuning noise: The Mute signal from Tu-μP was shifted from 5V to 9V signal. However, in VT-1310A/1305A, the Mute signal for defeating tuning noise from Tu-μP is supplied to the Automatic Gain Control circuit in Audio Processing circuit. The Line Mute Signal from S-μP is added to this signal by a diode adder circuit.
3. Reset Signal. In VT-1100A 1105A, $\overline{\text{RESET}}$ signal from REG/BAND SELECTOR IC to reset the μPs during a power source failure was added to Tu-μP directly and also added to S-μP through an Inverter Q804. However in VT-1310A/1305A, REG/BAND SELECTOR IC has RESET and $\overline{\text{RESET}}$ signals for both μPs.
4. 5.0V Output. In VT-1100A/1105A, the 5V Regulator Q808 supplies A5V to TUNING, SYSTEM CONTROL and etc. circuits. However, in VT-1310A/1305A, REG/BAND SELECTOR IC includes an A5V source.
5. Current Source. In VT-1100A/1105A, the 30V source for VT signal was supplied from current source Q811 and Zener diode ZD801. However, in VT-1310A/1305A, REG/BAND SELECTOR IC also includes a current source circuit for the same purpose.

6-4 VT-1310A/1305A AUDIO CIRCUIT

The audio circuit configuration of the VT-1310A/1305A is very similar to the VT-1100A/1105A. New audio processing IC M5165P which consists of LINE/TUNER input switch, ALC, REC/PB/LINE amp, SP-EQ switches and bias switch is used.

Fig. 6-7 shows the record audio processing circuit and Fig. 6-8 shows the playback audio processing circuit.

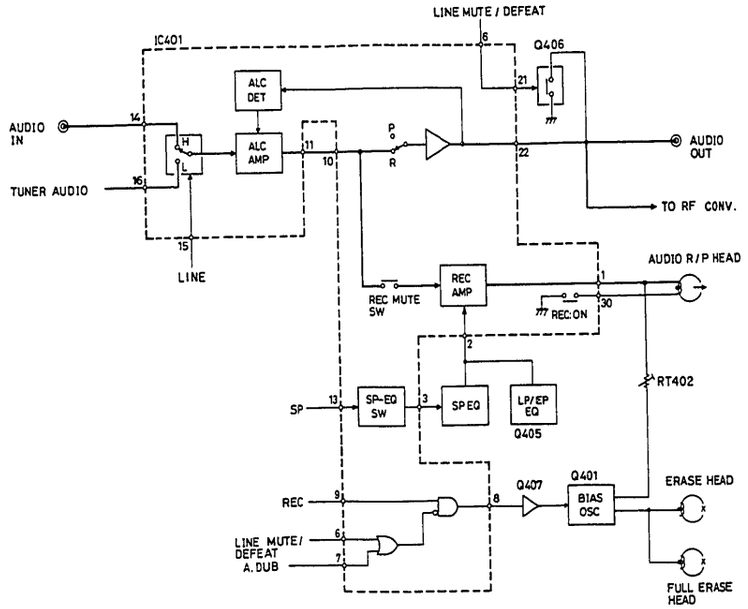


Fig. 6-7 Record Audio Processing Circuit

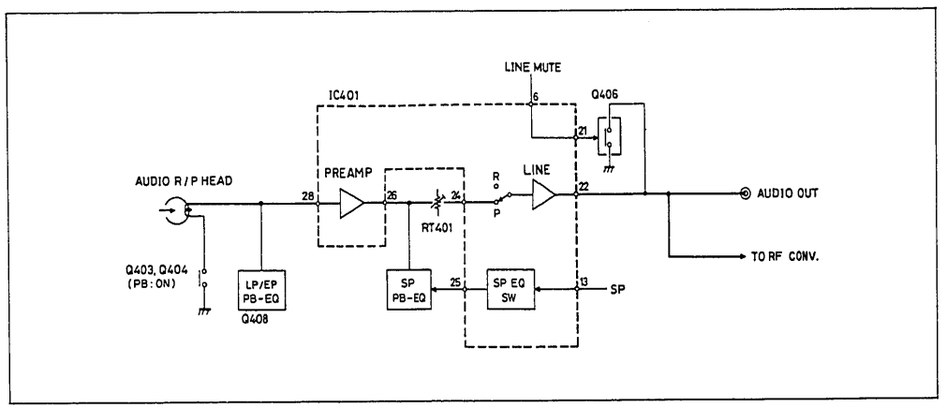


Fig. 6-8 PB Audio Processing Circuit

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VT-1100AR/1105A

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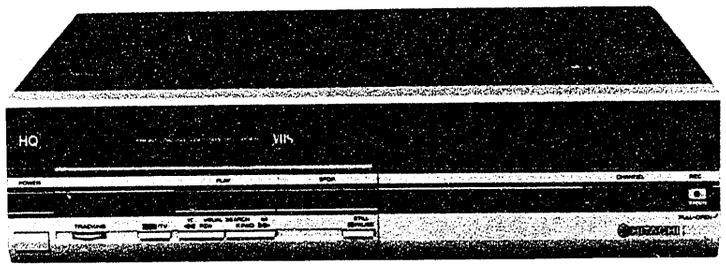
SERVICE MANUAL

TK **No. 2438E**

VT-1100AR/1105A

Technical Data



VHS

THIS VIDEO DECK IS A VHS TYPE VIDEO RECORDER.
FOR PROPER OPERATION, ONLY THE VHS TYPE CASSETTE MUST BE USED.

VT-1100AR/1105A

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

VIDEO CASSETTE RECORDER

April 1986 **TOKAI WORKS**

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SAFETY PRECAUTIONS

NOTICE: Comply with all cautions, and safety related notes located on or inside the cabinet and on the chassis.

1. When replacing a chassis in the instrument, all the protective devices must be put back in place, such as barriers, non-metallic knobs, adjustment and compartment convershields, isolation resistor-capacity, etc.
2. When service is required, observe the original lead dress. Extra precaution should be taken no assure correct lead dress in the high voltage circuit.
3. Always use the manufacturer's replacement components. Especially critical components as indicated on the circuit diagram should not be replaced by other manufacture's. Furthermore where a short circuit has occurred, replace those components that indicate evidence of overheating.
4. Before returning a instrument to the customer, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock, and be sure that no protective device built into the instrument by the manufacturer has become defective, or inadvertently defeated during servicing.

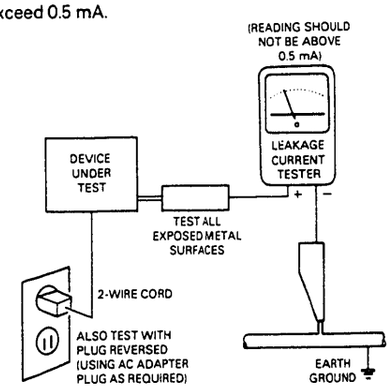
Therefore, the following checks should be performed for the continued protection of the customer and service technician.

Leakage Current Cold Check

With the AC plug removed from the AC120V, 60 Hz source, place a jumper across the two plug prongs. Turn the AC power switch on. Using an insulation tester (DC500V), connect one lead to the jumpered AC plug and touch the other lead to exposed metal part (antennas, screwheads, metal overlays, control shafts, etc.), particularly any exposed metal part having a return path to the chassis. Exposed metal parts having a return path to the chassis should have a minimum resistor reading of 0.3 MΩ and a maximum resistor reading of 5 MΩ. Any resistor value below or above this range indicates an abnormality which requires corrective action. Exposed meter parts not having a return path to the chassis will indicate an open circuit.

Leakage Current Hot Check

Plug the AC line cord directly into a AC120V, 60 Hz outlet (do not use an isolation transformer for this check). Turn the AC power switch on. Using a "Leakage Current Tester", Measure for current from all exposed metal parts of the cabinet (antennas, screwheads, metal overlays, control shaft, etc.), particularly any exposed metal part having a return path to the chassis, to a known earth ground (water pipe, conduit, etc.). Any current measured must not exceed 0.5 mA.


(READING SHOULD NOT BE ABOVE 0.5 mA)
LEAKAGE CURRENT TESTER
DEVICE UNDER TEST
TEST ALL EXPOSED METAL SURFACES
2-WIRE CORD
ALSO TEST WITH PLUG REVERSED (USING AC ADAPTER PLUG AS REQUIRED)
EARTH GROUND

AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE RECEIVER TO THE CUSTOMER.

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts have special safety-related characteristics. These are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by making with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the HITACHI recommended replacement one, shown in the parts list in this Service manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current HITACHI Service Manual. A subscription to, or additional copies of, HITACHI Service Manual may be obtained at a nominal charge from HITACHI SALES CORPORATION.

FOR CANADA

CAUTION AGAINST FUSE REPLACEMENT

FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH SAME TYPE AND SAME RATING FUSE IN ACCORDANCE WITH THE FUSE SYMBOL LABEL.

The following is the indication of the fuse symbol label which is affixed adjacent to the fuse in the equipment.

* Example

This symbol indicates Fast Operating Typ 2A, 250V Fuse.

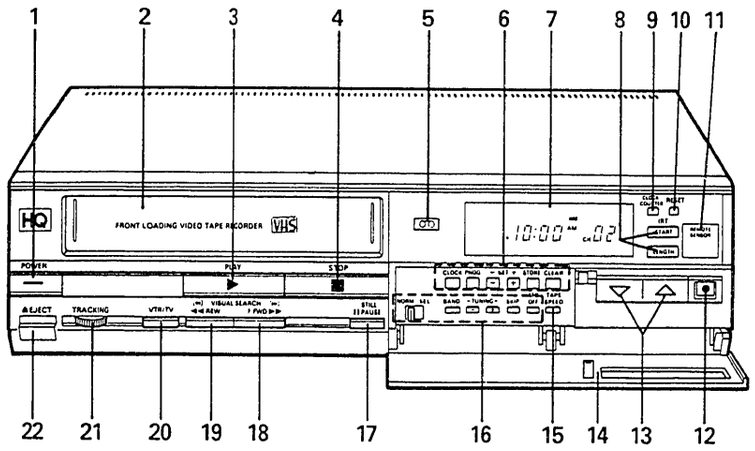
SPECIFICATIONS

ITEM	VT-1100AR/1105A
Recording:	Rotary two head Helical Scan Azimuth Recording
Video:	NTSC Color EIA Standard
Cassette:	VHS Type
Heads:	2 video heads: 2 for SP/LP/EP 1 Full track audio/video erase head 1 Combination head for control track, audio erase and audio record/play (3 heads/single housing)
Tape Speed:	33.35 mm/sec (SP), 16.67 mm/sec (LP), 11.12 mm/sec (EP)
Tape Width:	12.7 mm
RF Output:	Channel 3 or Channel 4
RF Input:	VHF 75 ohm, UHF 300 ohm
Tuning Range:	VHF LOW, CH2 ~ 6 (54 MHz – 88 MHz) VHF HIGH, CH7 ~ 13 (174 MHz – 216 MHz) VHF MID. CH A-2, A-1 and A ~ I (108 MHz – 174 MHz) CATV VHF SUPER CH J ~ W (216 MHz – 300 MHz) CATV UHF CH, 14 ~ 83 (470 MHz – 890 MHz)
Video Input:	1 – 2 Vp-p 75 ohm Unbalanced
Video Output:	1 Vp-p 75 ohm Unbalanced
Audio Input:	316 mV rms (–7.8 dB) 100 kohm
Audio Output:	316 mV rms (–7.8 dB) 600 ohm
Video Recording S/N:	Better than 46 dB (SP), Better than 43 dB (LP), Better than 40 dB (EP)
Horizontal Resolution:	240 lines (SP), 230 lines (LP), 230 lines (EP)
Audio Response:	50 Hz – 10 kHz (SP), 50 Hz – 7 kHz (LP), 100 Hz – 6 kHz (EP)
Audio S/N:	Better than 43 dB (SP), Better than 40 dB (LP), Better than 40 dB (EP)
Power Input:	AC 120V 60 Hz (VT-1100AR) AC 100~250V, 50/60 Hz (VT-1105A)
Power Consumption:	32W Nominal (VT-1100AR) 30W Nominal (VT-1105A)
Cabinet Size:	17-1/8"(W) x 3-3/4"(H) x 12-3/4"(D) 43.5(W) x 9.5(H) x 32.4(D) cm
Weight:	17.2 lbs (7.8 kg) (VT-1100AR) 13.7 lbs (6.2 kg) (VT-1105A)
Accessories:	1 – Coaxial cable with antenna adaptor 1 – UHF twin lead 1 – Matching transformer 300 – 75 ohm 1 – Remote control unit 2 – Batteries

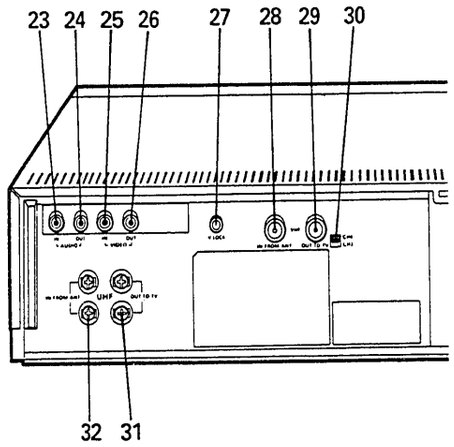
Design and Specifications subject to change without notice.

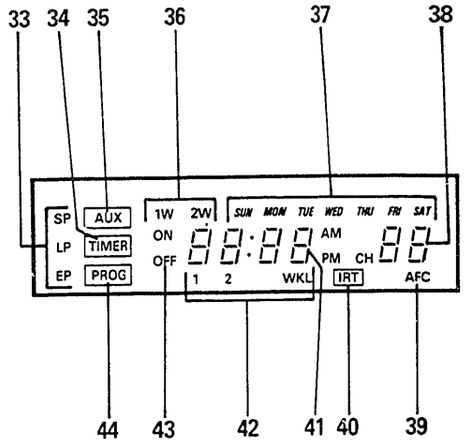
LIST OF DIFFERENCES

	ITEM		VT-1100A	VT-1100AR/1105A
FEATURES	HQ (HIGH QUALITY)		USED	USED
	TRICK PLAY		○ VISUAL SEARCH ○ STILL (FIELD)	○ VISUAL SEARCH ○ STILL (FIELD)
	AUTO POWER ON FUNCTION		YES	YES
	NOISE LOCK SEARCH FUNCTION		YES	YES
	REMOTE CONTROL		WIRELESS	WIRELESS
	TIMER RECORDING PROGRAMS		2 PROGRAMS/2 WEEKS	2 PROGRAMS/2 WEEKS
	TIMER BACKUP POWER		ABOUT 1 SECOND	ABOUT 1 SECOND
	TIMER PROGRAMMED TIME DISPLAY		START AND STOP SEQUENTIALLY	START AND STOP SEQUENTIALLY
	IRT		CAN SET START TIME	CAN SET START TIME
	TAPE COUNTER INDICATOR		CLOCK/COUNTER SWITCHING	CLOCK/COUNTER SWITCHING
	MEMORY STOP OPERATION MODE		REWIND AND F.FORWARD	REWIND AND F.FORWARD
	CHANNEL TUNING FUNCTION		VOLTAGE SYNTHESIZER	VOLTAGE SYNTHESIZER
	INPUT SELECT SWITCH		NONE	NONE
	PLAYBACK PICTURE CONTROL		NONE	NONE
	ONE BUTTON RECORDING		YES	YES
CHASSIS	BASIC CHASSIS TYPE		UY	UY
	CYLINDER MOTOR		THREE-PHASE OUTER ROTOR FG: 360 Hz	THREE-PHASE OUTER ROTOR FG: 360 Hz
	VIDEO HEAD		2 HEAD CH-1/CH-2: 30 μm CONNECTOR TYPE	2 HEAD CH-1/CH-2: 30 μm CONNECTOR TYPE
	HEATER		NONE	NONE
	DEW SENSOR		YES	YES
MAIN CONTROL ICs	VIDEO SYSTEM	Y-SIGNAL PROCESS CHROMA SIGNAL PROCESS REC/PB AMP AND CORRECTOR PICTURE CONTROL	HT4705C (IC201) HA11856 ANT (IC202) HT4723 (IC205) HA11852 (IC1) HT4723 (IC205)	HT4765C (IC201) HT4706A (IC202) HT4763 (IC205) HA11852 (IC1) HT4763 (IC205)
	AUDIO SYSTEM	REC/PB AMP	BA5119S (IC401)	M51654P (IC401)
	SERVO SYSTEM	SPEED/PHASE CONTROL CYLINDER MOTOR DRIVE CAPSTAN MOTOR DRIVE TRICK PLAY CONTROL	HA11853 ANT (IC601) HA13403 (IC1651) M54648L-B (IC602) ——	HA11853 ANT (IC601) HA13403 (IC603) M54648L-B (IC602) ——
	SYSTEM CONTROL	SYSTEM CONTROL μP LOADING MOTOR DRIVE	HD614042SD76 (IC901) M54649L (IC902)	HD614042SE43 (IC901) M54649L (IC902)
	TIMER	TIMER μP	M50752-635SP (IC751)	M50752-622SP (IC751)
	CH-TUNING SYSTEM	TUNING μP BAND SWITCHING	M50161-452SP (IC801) LA7934 (IC802)	M50161-454SP (IC801) LA7935 (IC802)
	POWER SUPPLY	REGULATOR	STK5471 (IC851)	STR11006 (IC851) VT-1105A STK5471 (IC851) VT-1100AR



1. **POWER SWITCH**
   Turn system power on and off.
2. **CASSETTE COMPARTMENT**
3. **PLAY BUTTON**
   Press to start play.
4. **STOP BUTTON**
   Press to stop tape. The STOP button must be pressed between "RECORD" and any other operation.
5. **TAPE-IN INDICATOR**
   Lights when cassette is located in the compartment.
6. **TIMER CONTROLS**
7. **ELECTRONIC DIGITAL DISPLAY**
   See next page for details.
8. **INSTANT RECORDING TIMER BUTTONS (IRT)**
   IRT allows unattended recording without programming the timer.
9. **CLOCK/COUNTER SELECT BUTTON**
   Press to select clock display or counter display.
10. **COUNTER RESET BUTTON**
    To reset counter to "0000".
11. **INFRARED RAY RECEIVING SECTION**
    Receives the infrared ray from remote control unit.
12. **RECORD BUTTON**
    Press to start recording.
13. **CHANNEL SELECT BUTTONS**
    Select the channels you wish to view or to record by pressing these buttons.
    And you can also select "AUX" by pressing these buttons to record or watch the program input at the VIDEO IN and AUDIO IN.
    (One channel position either higher or lower outside the range of your preset channels.).
14. **DOOR FOR SECONDARY CONTROLS**
15. **TAPE SPEED SELECT SWITCH**
    Recording time using Cassette tape T-160:
    EP: 8 hours
    LP: 5.3 hours
    SP: 2.6 hours
    Note: Playback speed automatically corresponds with recorded speed.
16. **CHANNEL PROGRAMMING CONTROLS**
    Program channels for channel up and down selection with these controls.
17. **PAUSE/STILL BUTTON**
    Press to pause during recording or playback.
18. **FAST FORWARD/VISUAL SEARCH BUTTON**
    Press to activate fast forward.
    Press this button during playback of a recorded tape, and forward playback picture at high speed can be seen.
19. **REWIND/VISUAL SEARCH BUTTON**
    Press to start rewind.
    Press this button during playback of a recorded tape, and reverse playback picture at high speed can be seen.
20. **VTR/TV SELECT SWITCH**
    Selects the signal to be viewed.
    The VTR indicator comes on when the unit is in VTR mode and the signal received by the VTR is displayed on the TV screen. With the switch in the TV position (indicator light off) the broadcast signal is received directly by your TV set. When the VTR power is turned off, the VTR automatically switches to "TV".
21. **TRACKING CONTROL KNOB**
    To minimize noise in playback.
22. **EJECT BUTTON**
    With power on, press to remove cassette.

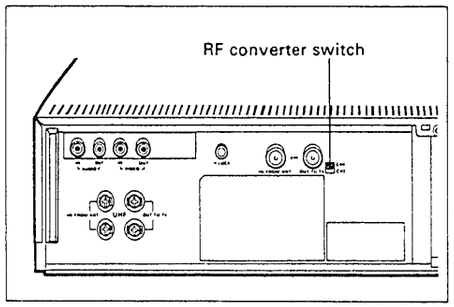




23. **AUDIO IN**
    Receives audio signals from a camera or from another VTR.
24. **AUDIO OUT**
    For a connection to a monitor or another VTR.
25. **VIDEO IN**
    Receives video signal from a video camera or another VTR.
26. **VIDEO OUT**
    For connection to monitor TV.
27. **V. LOCK**
    Use to minimize vertical jitter during still playback.
28. **VHF ANTENNA INPUT**
    Connect the VHF antenna to this terminal.
29. **VHF ANTENNA OUTPUT**
    Connect this terminal to the VHF antenna terminal on the back of the TV.
30. **RF CONVERTOR SWITCH**
    Set this switch to whichever channel (CH3 or CH4) is unused in your area.
31. **UHF ANTENNA OUTPUT**
    Connect these terminals to the UHF antenna terminals on the back of the TV.
32. **UHF ANTENNA INPUT**
    Connect the UHF antenna to these terminals.
33. **TAPE SPEED INDICATORS**
34. **TIMER INDICATOR**
    Will light when turning power off after programming.
35. **AUX INDICATOR**
    Will light when the AUX position is selected by pressing the channel select buttons. AUX position is used to record or watch the program input at the VIDEO IN and AUDIO IN.
36. **WEEK INDICATORS FOR TIMER RECORDING**
    1W: Up to seven days from the present day.
    2W: Eighth day to fourteenth day from the present day.
37. **DAY INDICATORS**
    Normally shows the current day of week. Shows the recording start day when programming the timer.
38. **CHANNEL INDICATOR**
39. **AFC INDICATOR**
    Shows that Automatic frequency control (AFC) circuit turns on.
40. **IRT INDICATOR**
    Lights during Instant recording.
41. **CLOCK/TAPE COUNTER DISPLAY**
    Normally shows the present time or tape counter. Shows time remaining during Instant recording.
42. **PROGRAM DESIGNATION FOR TIMER RECORDING**
43. **ON/OFF INDICATORS FOR TIMER RECORDING**
    ON shows recording start time.
    OFF shows recording stop time.
44. **PROG INDICATOR FOR TIMER RECORDING**
    Lights if any program is in the timer.

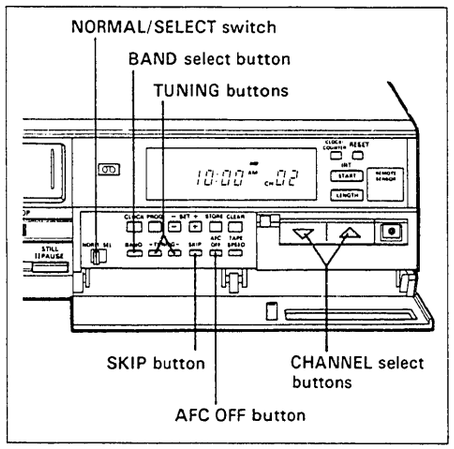
VIDEO CHANNEL SETTING

The RF converter changes the video and audio signals from the tuner or tape playback, to a standard television broadcast signal on channel 3 or 4. To obtain video recorder output on either channel 3 or 4, set the RF converter switch to CH 3 or 4 whichever channel is unused in your area.



CHANNEL TUNING

Your VTR can be preset for up to 80 memorized channels. It has been preset to receive VHF channels 2 through 13 when shipped. The channel number in the display will originally match the actual TV channel selected. During the procedure which follows, you can reprogram any display channel number, so that it selects any actual TV channel. This means that after programming of the memorized channels, the display can indicate a different number than the actual TV channel tuned by that channel memory position.
You can set any channel memory position to receive any station. This ability is most useful when the tuner is used in CATV installations. To add UHF or CATV channels not factory preset, or to preset the VHF channels in some other order, use the procedure which follows.



1. Turn on the TV and VTR.
2. Set the TV to Channel 3 (or 4).
3. Set the RF converter switch of VTR to channel 3 (or 4).
4. Open the door for secondary controls.
5. Set the NORMAL/SELECT switch to "SELECT". Time indication will change to band indication.
   Note: When the switch is set to "SELECT", the display should indicate the band indication. If not, turn off VTR power, and then turn it on again to indicate the band indication.
6. Select the channel number to be memorized by pressing the CHANNEL select buttons.
   Note:
   1. Your VTR can use the following numbers as TV channel presets: 00, 01 through 72, 91, 92, 95 through 99.
   2. Your VTR has been preset to receive VHF channels 2 through 13.
   3. You should determine which channel memory positions have not been preset before entering programming information. New information automatically erases previous programmed data.
7. Press the BAND select button to select either "L", "H" or "U" according to the channel number as listed below.

Indication on display	Channnels to be received	
L	VHF low channels	2~6
H	CATV channels VHF high channels CATV channels	A-2, A-1 and A~I 7~13 J~W
U	UHF channels	14~83

For example, if you're going to tune one of UHF channels 14 through 83, display the letter "U" by pressing the BAND select button.

8. Press and hold the TUNING button (+) until the picture for the channel number you are programming appears on the TV screen. (For fine tuning tap on the "+" and "−" TUNING button alternately.) The active channel with lowest number in the band being programmed will appear, followed in order by the other active channels, as in the "Channel frequency spectrum" on next page.
   Note:
   1. Holding down the TUNING button (+) at the end of band will result in tuning into the next band. The band display will change to the next higher band.
   2. If you press the TUNING button (−) at first, the band will change to adjacent band immediately. The active channel with the highest frequency in the band will first appear, followed in opposite sequence by the other active channels.
   3. Speeds of picture scanning from the lowest channel to the highest in each band are as follows;

Band	Speeds
L	About 20 seconds
H	About 40 seconds
U	About 80 seconds

9. After releasing the TUNING button when the channel picture appears for the channel number you are programming, press the up (+) and down (−) TUNING buttons to fine tune the TV channel.
10. Repeat steps 6 through 9 for other channels.
11. Return the NORMAL/SELECT switch to "NORMAL".
12. To check programming, press the CHANNEL select buttons to cycle the VTR tuner through all the channels you have programmed. If a channel was missed or requires fine tuning, repeat above steps for the channel involved.

Always return the NORMAL/SELECT switch to "NORMAL" after preprogramming is complete.

AFC (Automatic Frequency Control)

A channel is fine tuned using up (+) and down (−) SEARCH buttons. When the NORMAL/SELECT switch is returned to "NORMAL", AFC is turned on and the channel "locks in". The AFC electronically optimizes the fine tuning adjustment.
If a TV channel signal is marginal due to graininess or ghosting, the picture may sometimes be improved by manually tuning for best picture and then defeating the AFC action. To turn AFC off, follow the procedure below.

AFC off tuning procedure

1. Make sure that NORMAL/SELECT switch is set to "NORMAL".
2. Select the desired channel by pressing CHANNEL select button.
3. Set the NORMAL/SELECT switch to "SELECT".
4. Press the AFC OFF button.
   "AFC" indication under the channel indication display will disappear.
5. Return the NORMAL/SELECT switch to "NORMAL".
   Note:
   1. The AFC is only switched off for the channel you have been programming. AFC remains in effect on all other channels. To defeat the AFC for additional channels, repeat the above steps.
   2. Pressing the AFC OFF button once again will turn the AFC on.

Eliminating unwanted preset channels

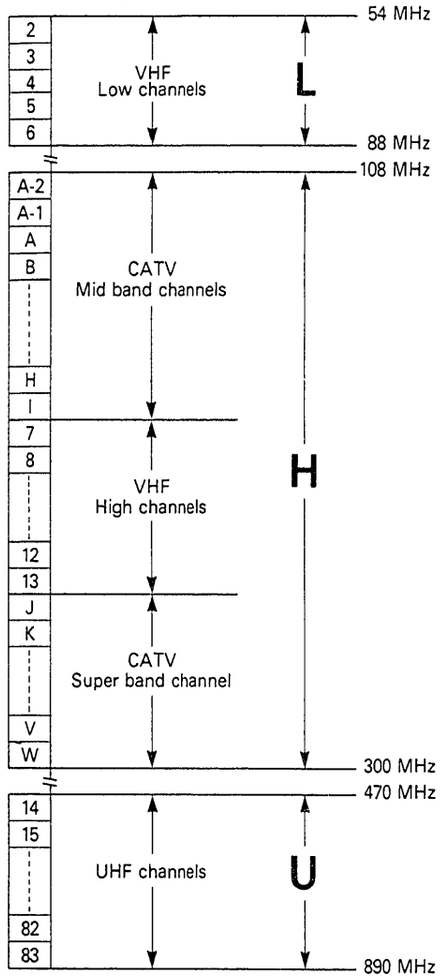
You can rearrange the desired channels by eliminating unwanted preset channels for channel up/down selection.

1. Set the NORMAL/SELECT switch to "SELECT".
2. Press the CHANNEL select buttons until an unwanted channel is tuned.
3. Press SKIP button.
   Sound will go off indicating the channel has been erased from memory.
4. Repeat steps 1 through 3 until all unwanted channels have been eliminated.
5. Return the NORMAL/SELECT switch to "NORMAL".

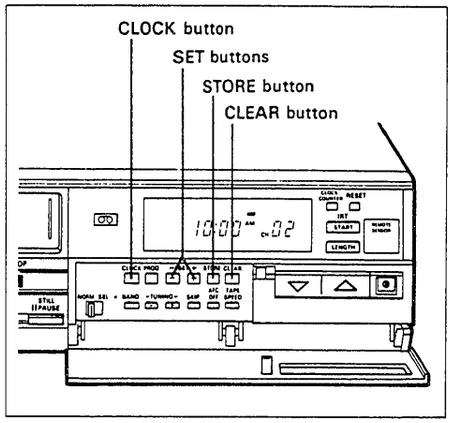
Channels which have been eliminated cannot be selected by the CHANNEL select buttons.
Note: To restore the erased channel, repeat the above steps 1 through 3.

> Your VTR has been preset to select the "AUX" position by pressing the CHANNEL select buttons.
> This AUX position is used to view or record the program input at the VIDEO IN and AUDIO IN on back of VTR.
> The "AUX" position can be eliminated for channel up/down selection and also can be re-entered in memory by following the steps 1 through 3 on "Eliminating unwanted preset channels".

Channel frequency spectrum



CLOCK TIME SETTING



- When VTR is plugged into an AC outlet for first time, the clock display shows "– – : – –".

The clock is set using the CLOCK, SET and STORE buttons. The CLOCK button selects the clock setting mode. The SET buttons advance the Day, Hours or Minutes. The STORE button stores the Day, Hours or Minutes. After the Day is entered with STORE, the next press of the STORE button will enter the hours, and next press will enter the minutes. To indicate the "DAY" mode, the day will flash. To indicate the "HOUR" mode, the hours digits will flash. To indicate the "MINUTE" mode, the minutes digits will flash. When the STORE button is pressed, the flashing digits will be stored in memory.
If you input erroneous information by mistake during clock setting, press the CLEAR button then input correct information again.

Before setting the clock, program your VTR tuner.

1. Press the CLOCK button.

2. Press the SET button (+ or –) repeatedly to select the present day of the week.
   Hold the button down to advance rapidly.
   When the present day of the week appears, press the STORE button.

For example, the diagram shows that Saturday (SAT) has been set.

3. Press the SET button (+ or –) to set the present hour.
   Hold the button down to advance rapidly. Press the STORE button when the present hour appears.

For example, the diagram shows that "AM 10" hour has been set.

4. Press the SET button (+ or –) to set the minute.
   Hold the button down to advance rapidly. Press the STORE button when the present minute appears.

For example, the diagram shows that "30" minutes has been set.

Now the clock has been set to the correct time of day.

For zero second setting, set the minutes to one minute ahead of present time and press the STORE button when the exact start of the next minute is reached.

Note:
- If your clock display shows "– – : – –", your home had a power failure. The time should be reset.
- 12:00 AM is midnight; 12:00 PM is noon.

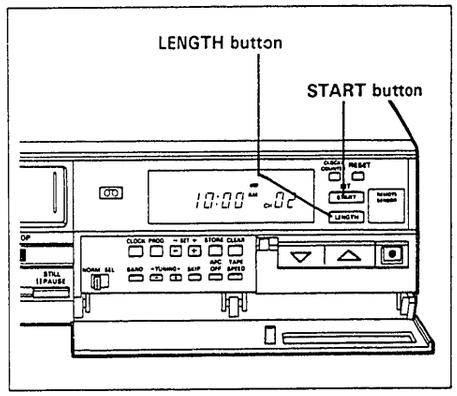
NORMAL TV VIEWING

You do not need to disconnect VTR from your TV set to watch TV. When you turn off the POWER switch on your VTR, the VTR automatically switches to "TV".

To watch TV, turn on TV and select a channel as usual.

INSTANT RECORDING

Instant recording timer (IRT) allows you to start an unattended recording without programming the timer.
It is convenient if you are interrupted while viewing a program and want to record the balance of it.
By using the delayed start feature you can delay the recording start up to 24 hours. Although you do not need to program the timer for IRT, the clock must be set.



IRT with immediate start

1. Follow the steps 1 through 5 on "RECORDING TV PROGRAM".
2. Press the LENGTH button to select the recording time. Pressing the button once sets the timer to "0:00". The recording time changes in hour and minute in the order of 0:30, 1:00, 1:30, 2:00, 3:00 and 4:00 every time the button is pressed. IRT will begin when 0:30 is displayed and the TIMER and IRT indicators will come on. During recording, the remaining IRT time appears on the timer display.
3. At the end of recording the display reads 0:00; the VTR will automatically shut off.

Note:

1. IRT feature does not operate during play and unattended recording modes.
2. If the LENGTH button is pressed during rewind operation, VTR enters the IRT mode after rewinding tape.

Delayed start IRT

You can delay the start of an IRT by using the START button.

1. Follow the steps 1 through 5 on "RECORDING TV PROGRAM".
2. Press the START button to set the start time.
   The start time may be set to begin on any hour or half hour, up to 24 hours from present.
   For example, the present time is 9:15 and you want to record a program that starts at 10:30. Just press the START button three times.

3. Press the LENGTH button repeatedly to select the desired recording time. The recording time changes in hour and minute in the order of 0:30, 1:00, 1:30, 2:00, 3:00 and 4:00 every time the button is pressed.
4. Turn off the VCR power.
   The TIMER indicator will come on, and IRT will begin at the time you selected.
   During recording, the remaining IRT time appears on the timer display.
   Note: Delayed IRT will not begin if the VTR is turned on at the start time.

Recalling the IRT

Press the START or LENGTH button only once to recall the start time or recording time respectively. The display shows start time or recording time for about 8 seconds and returns present time of day or counter reading.

Note: To recall the recording time, press the LENGTH button only once. If you press the button twice or more, the recording time will be changed.

To extend the recording time

The recording time can be extended anytime by pressing the LENGTH button. The timer display will reset to 0:30, 1:00, 1:30, 2:00, 3:00 or 4:00 as selected.

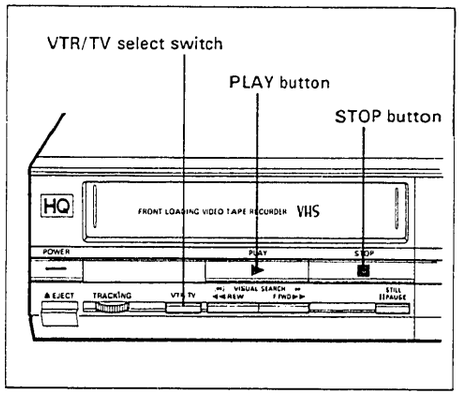
To cancel IRT

You can clear IRT by pressing the LENGTH button until time remaining is 0:00, or by pressing the POWER button and then the STOP button within 10 seconds.

Note:

1. When the recording is not taking place, press the LENGTH button until the display reads 0:00 to cancel IRT.
2. The presetting of IRT is not possible when the previous information is still stored.

PLAYBACK



1. Insert the cassette.
   VTR power is turned on automatically.
2. Turn the TV set on and select the video channel.
3. Set the VTR/TV select switch to "VTR". (VTR indicator lights.)
4. Press the PLAY button.
5. Press the STOP button to stop playback.

Tracking control adjustment

When playing prerecorded tapes or those recorded on units other than you own, black and white streaks may appear on your TV screen. If this occurs, turn the TRACKING control slowly in either direction until the streaks disappear. When playback of this particular tape is over, readjust the TRACKING control to its original position. The original position is normally in the center position.

Still playback

Press the PAUSE/STILL button to stop the picture on the screen during playback.

During still playback, press the PAUSE/STILL button to return to normal playback, or the STOP button to enter the VTR to the stop mode.

Note:

- If you see vertical shaking on the TV screen in the still playback mode, rotate the V. LOCK control on the back of the video deck to minimize shaking.
- When the still playback mode continues for about 5 minutes, the video deck switches to the stop mode automatically to prevent damage to the tape.
- The playback picture will have some noise in the still playback mode.

Visual search

This allows you to view the picture from a recorded tape at high speed in both the forward and reverse directions.

Press the PLAY button to play a tape, then press either the VISUAL SEARCH button REW or F.FWD. Pictures can be viewed at high speed in either the forward or reverse direction.

Note: The playback picture will have some noise in the visual search mode.

Automatic rewind

The tape will stop and automatically rewind when the end of the tape is reached.

This function does not operate during Timer recording and Instant recording.

Rewind shut off

If power switch is pressed during rewind operation, power will be turned off automatically after the tape has been completely rewound.

Tape counter

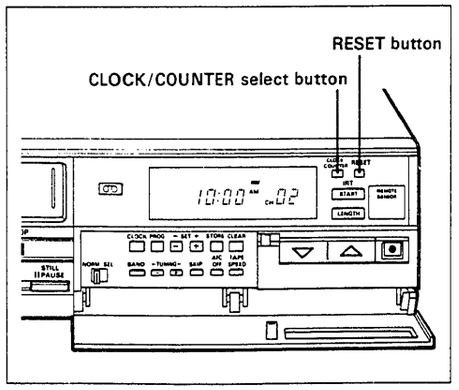
This indicates the amount of video tape transported as a number.

Press the CLOCK/COUNTER select button to indicate the counter reading on the display. Then press the RESET button to set the counter reading to "0000" when starting recording or playing back.

Note the number on the Tape counter at the beginning and end of each program you record. This will allow you to use the counter to find the desired program later.

Counter memory function

This is useful if there is a section of tape you want to view immediately after recording or you want to return to the same point several times.



1. Press the CLOCK/COUNTER select button and indicate the counter reading.
2. Begin recording or playing back a tape.
3. At the point where you want playback to begin, reset the tape counter to "0000" by pressing the RESET button.
4. Continue to play or record.
5. Press the STOP button when recording or playback finishes.
6. Press the REWIND button.

The tape will automatically stop at the pre-selected "0000" position.

Actually, so that you won't miss the very first part of the program to be viewed, the tape will stop slightly prior to "0000" at approximately the "9997" position.

Note:

1. With CLOCK/COUNTER select button in "CLOCK", counter memory will not operate.
2. The tape will also automatically stop at "0000" during fast forwarding.

REMOTE OPERATION

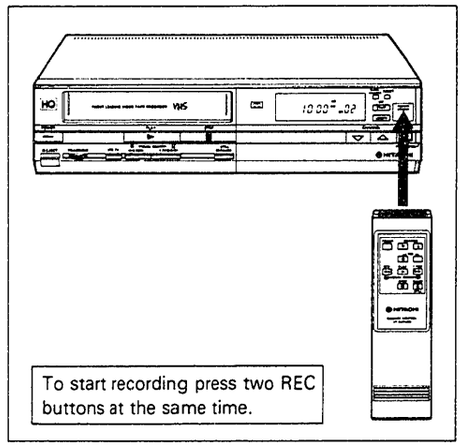
You can operate the VTR from a distance using the Infrared Remote Control unit.

Power source of infrared remote control unit

The infrared remote control unit is powered by two batteries (size AA). Insert the batteries (provided) so that their positive ends contact the positive terminals in the battery compartment. The life of the batteries is about one year although it depends on the number of times the unit is used. Replace the batteries when operation is not possible or when the distance becomes too small.

Operation of remote control

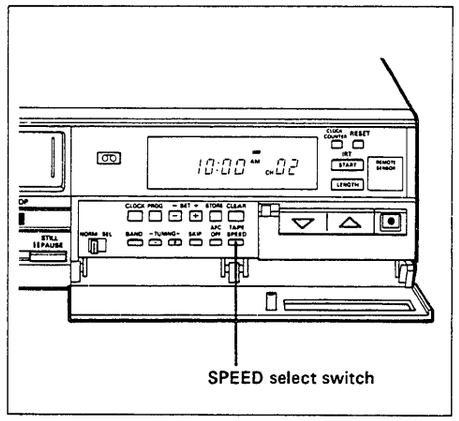
To use the infrared remote control unit aim it at the receiver on the front panel of the VTR.



Note: The infrared rays will bounce off the walls and eventually reach the receiver on the VTR, but for best results transmit rays directly to the receiver.

TIMER RECORDING

The programmable electronic clock/timer permits the unattended recording of up to 2 preselected programs, including one program on the same day of each week or one program at the same time Monday through Friday. It can be preset up to 14 days in advance to record your favorite programs. It turns the unit on and off and changes channels automatically.



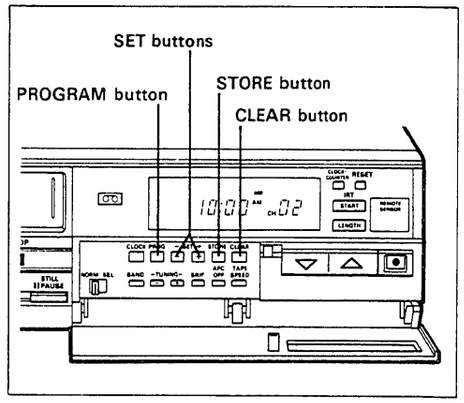
- Your TV does not have to be on to make a recording because the VTR records TV programs without the aid of your TV. Your TV is used only to view the program during recording or play.

1. Insert the Cassette.
2. Set the SPEED select switch to "SP", "LP" or "EP".
   Note: "SP" speed is recommended when recording a music program.
3. Set the program timer.
   "START (ON) TIME", "STOP (OFF) TIME", "DAY" etc. See below.
4. Turn power off. Now recording will begin automatically at the start time.

Note:

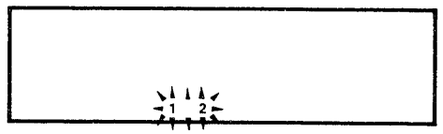
- It is not necessary to press RECORD button.
- The TIMER indicator flashes to warn that recording will not occur because cassette has not been inserted. If the safety tab on the cassette has been removed, the VTR will automatically eject the cassette when placed in the Timer mode.

Programming the timer for unattended recording
For unattended recording the timer needs to know what **day** to make the recording, the **time to start**, the **time to stop**, and the **channel to be recorded**.

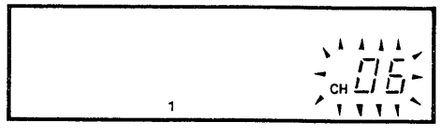


The timer is programmed using the PROGRAM, SET and STORE buttons. The PROGRAM button selects the timer programming mode. The SET buttons advance the Program indicators, Channel, Day, Hours or Minutes for recording. The STORE button stores them. The digits flash in sequence, so input the correct data to the flashing digits. When the STORE button is pressed, the flashing digits will be stored in memory.
If you input erroneous information by mistake when programming the timer, press the CLEAR button and input the correct information again.

1. Press the PROGRAM button.
   Program indicators (1 and 2) flash to indicate which memory positions have not been programmed. If a memory has been programmed, its indicator will not flash.
   Note: You should determine which memory positions have not been programmed before entering new programming information. New information automatically erases previous programming.

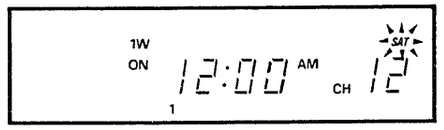


2. Press the SET button (+) to select the program indicator to be programmed. Program indicators (1 and 2) light alternately across bottom of digital display. Press the STORE button when the desired program number is displayed. Channel indicator starts flashing.



For example, diagram shows program "1" has been set.

3. Choose the channel to be recorded by pressing the SET or CHANNEL select button. Then press the STORE button.



For example, diagram shows channel "12" has been set.

4. Press the SET button to select the day of recording. Make sure desired Week indicator (1W or 2W) lights. Continuing forward will advance timer to Week two.
   Press the STORE button after selecting the day of recording. "AM 12" hour starts flashing.

For example, diagram shows recording on Thursday within 1 week from today.

To record on a specified day at the same time each week: Press the SET button until the "WKL" indicator lights and then press the SET button to select the day of recording. Then press the STORE button.

For example, diagram shows recording on Saturday of each week.

To record at the same time on Monday through Friday:
Press the SET button until Monday through Friday indicators light, then press the STORE button.

5. Select the hour for recording to start by pressing the SET button. Hold down button to advance rapidly. Advance hours for AM/PM. Press the STORE button after selecting the hour for recording to start.
   "00" minutes starts flashing.

For example, the diagram shows "AM 8" hours has been set.

6. Select the minutes for recording to start by pressing the SET button. Hold down button to advance rapidly. Press the STORE button after selecting the minute for recording to start.
   "OFF" will appear instead of "ON".
   "AM 8" hour starts flashing.

For example, the diagram shows "30" minutes has been set.

7. Select the hour and minute to stop recording in the same procedures described in steps 5 and 6. Be sure to press the STORE button after selecting the minute.

Programming of one timer event has now been completed. Display shows the start time when pressing the STORE button. After few seconds the display shows stop time, the display returns the clock time display together with letters "PROG" automatically.
"PROG" shows that timer has been programmed; it lights whenever the timer-programming is done regardless of whether the power ON/OFF. To set the next program, repeat steps 1 through 7.

Note: If a power failure occurs and the clock display shows "--:--", programming information previously set is cleared. The programming information should be reset.

To clear a program

1. Press the SET button (+) until desired program indicator lights. The start time appears on the display.
2. Press the CLEAR button.
   The display returns the clock time display to show that the programming has been cleared. Be sure to press the CLEAR button while the display shows the start or stop time. The programming does not clear if the CLEAR button is pressed when the display returns the clock time display.

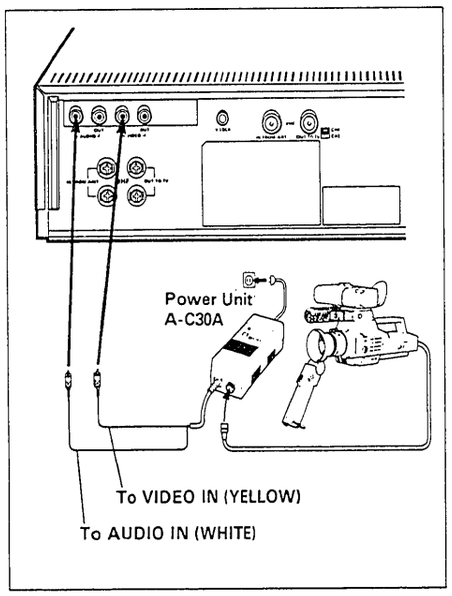
To stop a timer recording while in progress
Press the POWER button and then press the STOP button within 10 seconds.
The program that was being recorded will be erased from the timer's memory.

To check programming
Press the SET button (+).
The program indicator "1" lights. If the program No. 1 has been already programmed, the "ON" indicator lights and the clock/timer display shows the starting time. Then the "OFF" indicator lights and the display automatically shows the time to stop recording in a few seconds with the channel number to be recorded lighting up. The display then automatically returns to the present time of day.

Programming errors
If programs overlap, the video deck will select the program with the earliest start time. When that program is over, the video deck will switch to the next program. If the start times are the same, the video deck will select the programs in numerical order.

RECORDING FROM A VIDEO CAMERA

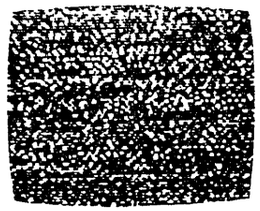
You will need a Video Camera and Power Supply for Video camera. At first you must connect the Video Camera to Power Supply and then connect Power Supply to Video Deck. (Refer to the Instruction Manual of the Camera as well as these instructions.)



1. Turn on Power Unit.
2. Insert cassette.
   VTR power is turned on automatically.
3. Set the SPEED select switch to "SP", "LP" or "EP"
4. Press the CHANNEL select button until the AUX indicator lights up on the display. If you have skipped the AUX position from the VTR tuner, restore it. See page 14 for details.
5. Adjust focus and white balance on camera. (Refer to Instruction Manual of video camera.)
6. Press RECORD button.
7. Press STOP button to stop recording.

HEAD CLEANING

- Picture playback may become blurred or be interrupted while the TV program received is clear. This does not mean that the recorded program has been erased. (See figure below.)
- Dirt accumulated on the head after long periods of use causes this problem. In this case, head cleaning requiring highly technical care is necessary.
- Video heads rotate rapidly and are easily damaged if they contact objects other than video tape. Under most conditions, they tend to be self cleaning due to contact with the tape. If the video heads become dirty, the picture will become snowy. Only when the picture becomes snowy and the tracking control has no effect, should the heads be cleaned.
  Head Cleaning Cassettes are available in the marketplace for customer use, but the quality and effectiveness of these Cleaning Cassettes ranges from satisfactory to poor. Some cleaning cassettes increase head wear or cause damage to the video heads. Others may become stuck in the machine. We recommend that head cleaning be performed only by qualified video recorder technicians. Head cleaning or malfunctions caused by head cleaning is not covered by the Limited Warranty.



Example of playback with dirty video heads

DISASSEMBLY

1. NAMES AND LOCATIONS OF CIRCUIT BOARDS

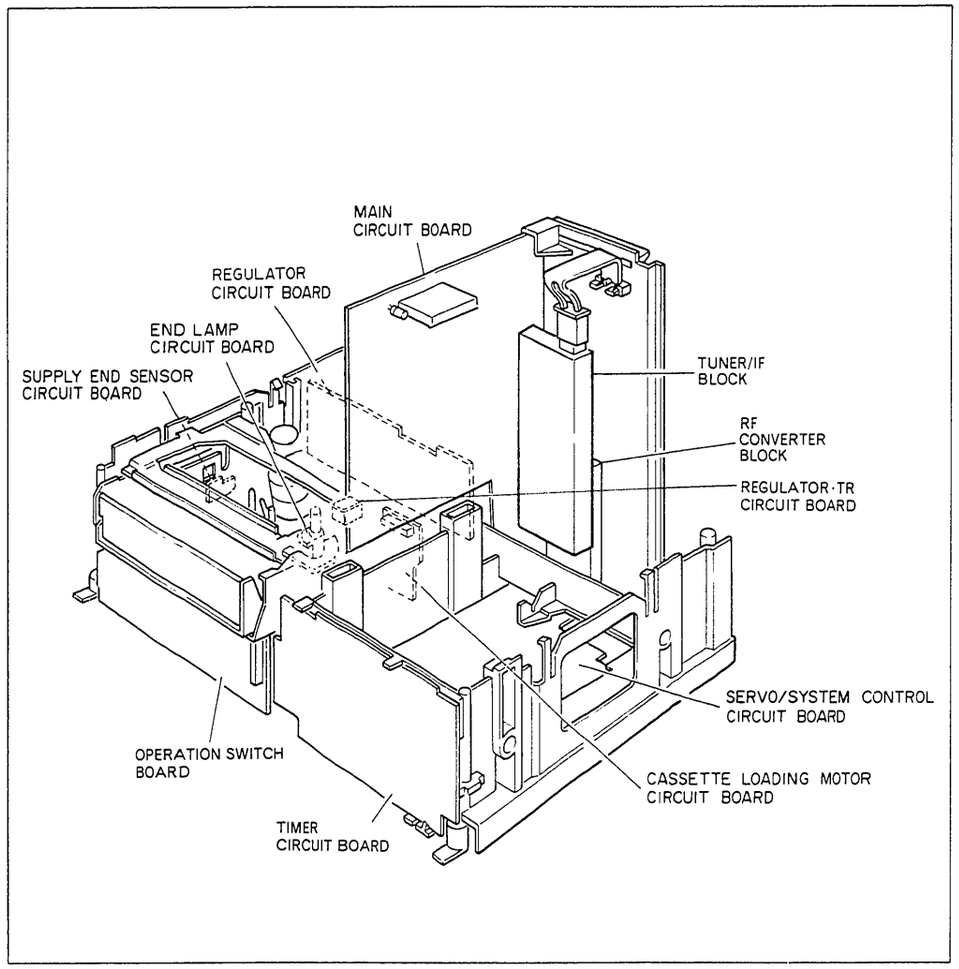


Fig. 1

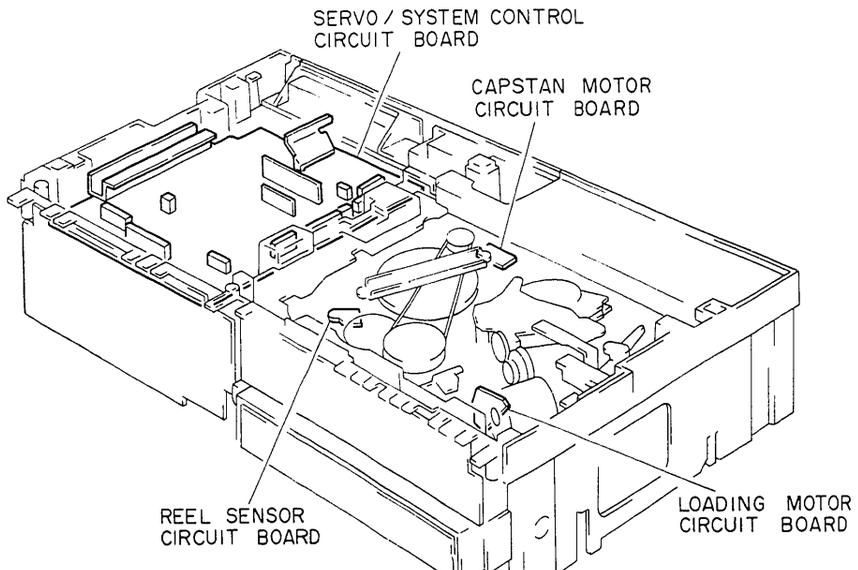


Fig. 2

(See page 2-8 for details on removing these circuit boards.)

2. NAMES AND LOCATIONS OF MAIN MECHANICAL COMPONENTS

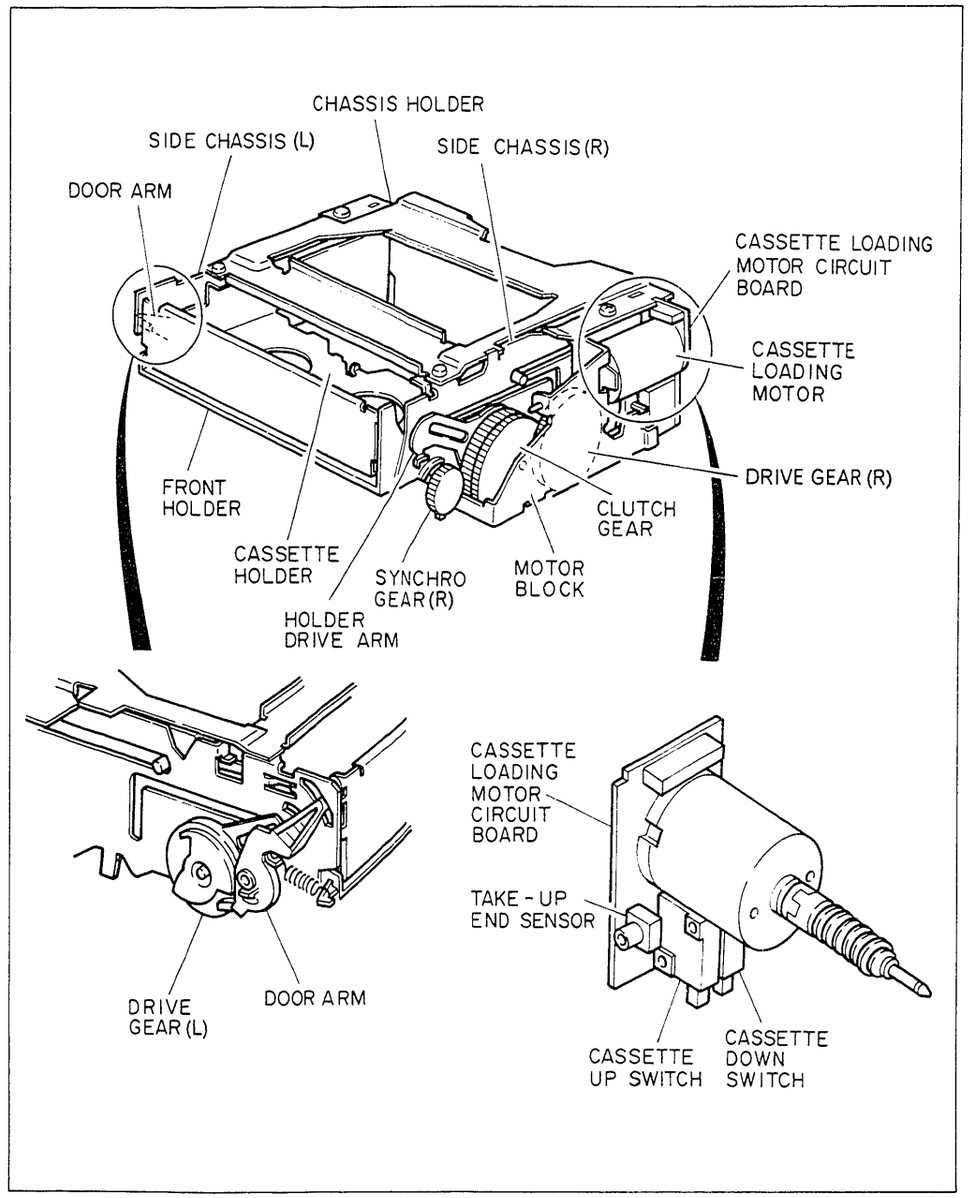


Fig. 3

(See page 2-10 for details on removing the above components.)

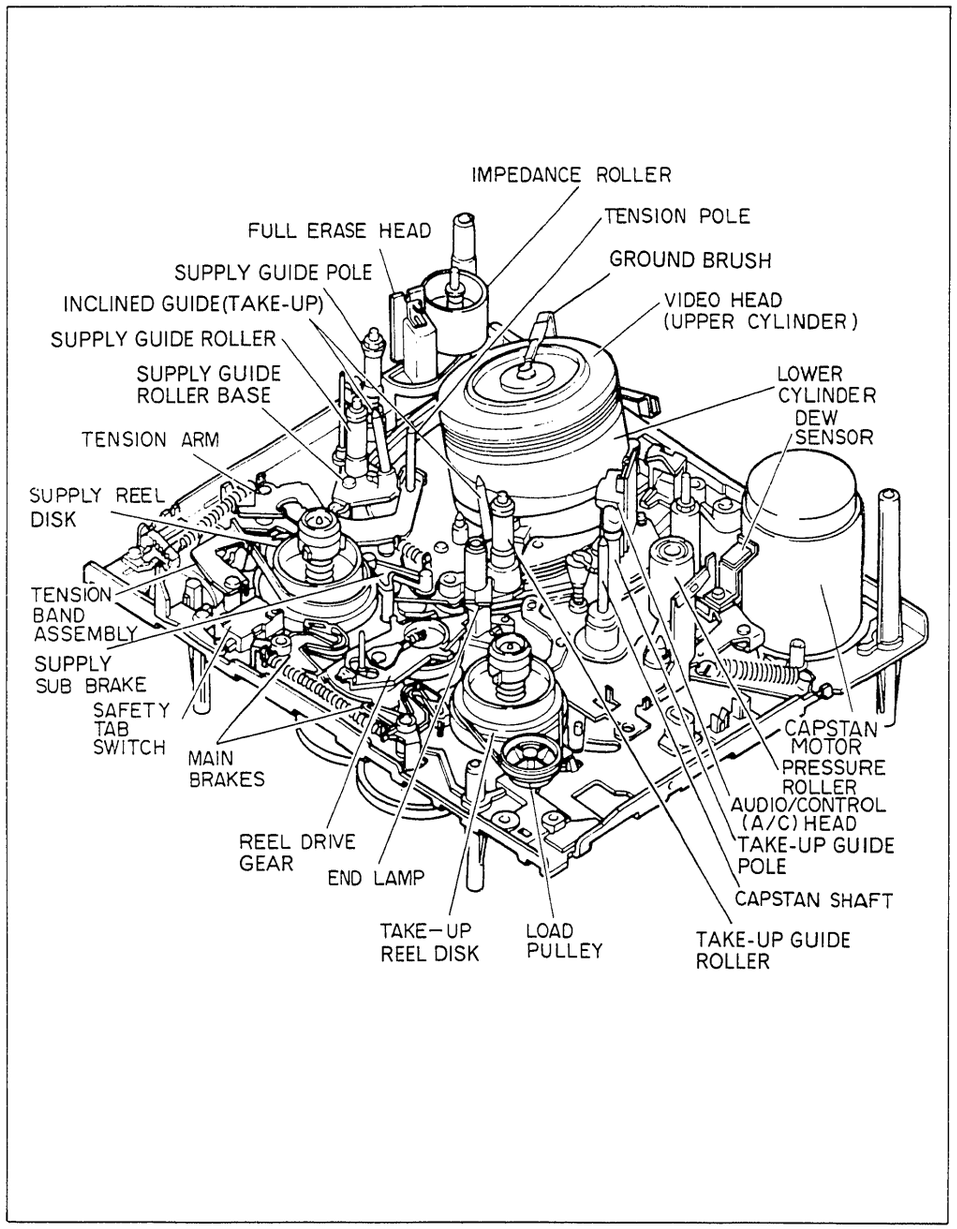


Fig. 4

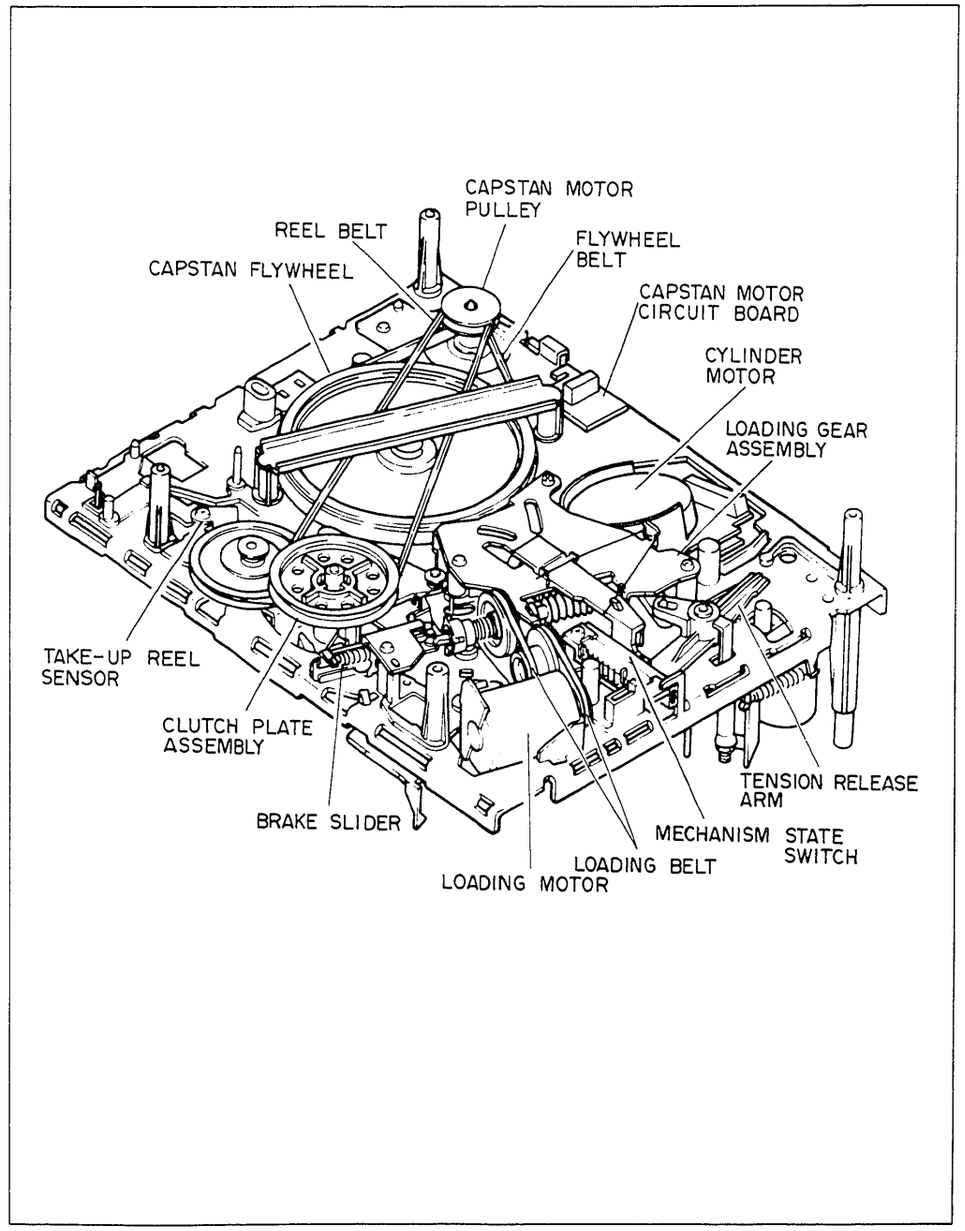


Fig. 5

(See page 2-13 for details on removing the above components.)

3. CASE REMOVAL

1. Preset door
2. Top cover
3. Bottom cover
4. Front panel
5. Rear panel
6. Remote controller

1. Preset Door

1) Open the preset door. Press down on the attachment holder and pull outward in the direction of the arrow.

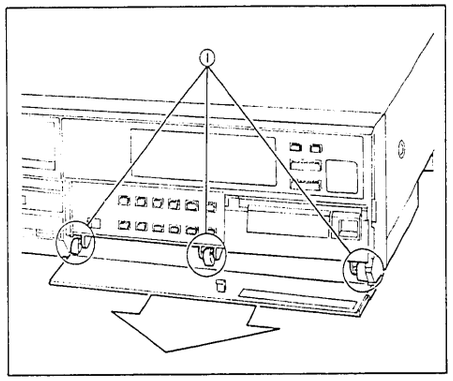


Fig. 1 Preset Door

2. Top Cover

1) Remove the 5 screws.
2) Lift the rear of the top cover upward. Slide the entire cover to the rear.

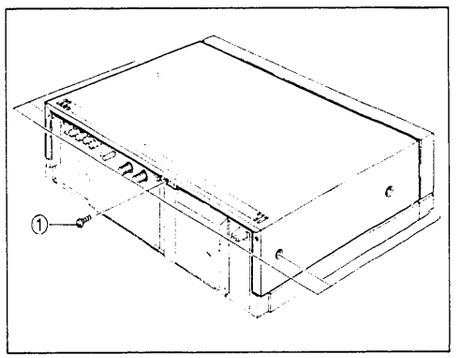


Fig. 2 Top Cover

3. Bottom Cover

1) Remove the 6 screws.

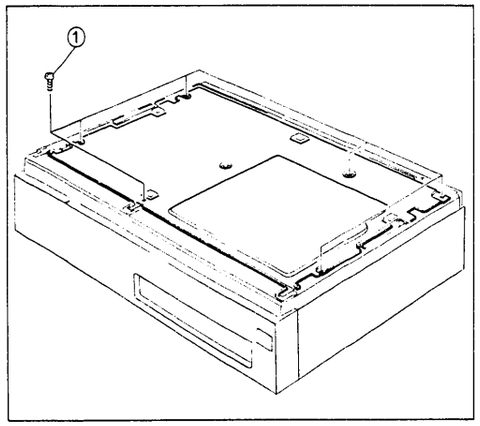


Fig. 3 Bottom Cover

4. Front Panel

1) Remove top and bottom covers (see items 2 and 3).
2) Remove the 4 screws.
3) Release the 8 stoppers.
4) Tilt the top toward you and pull out the entire front panel.

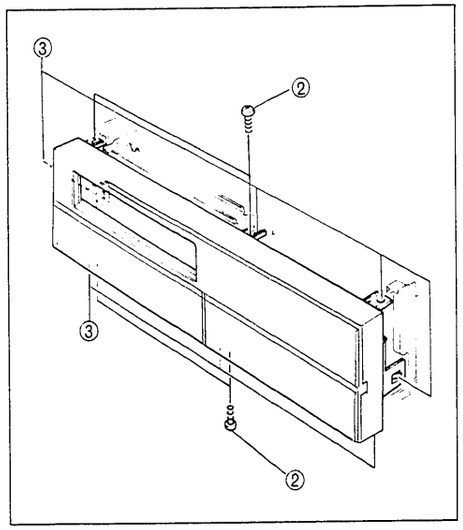


Fig. 4 Front Panel

5. Rear Panel

1) Remove the top cover (see item 2 in the section on case removal).
2) Remove the main circuit board (see item 1 in the section on circuit board removal).
3) Remove the screw.
4) Release the 2 stoppers.
5) Pull out the rear panel.

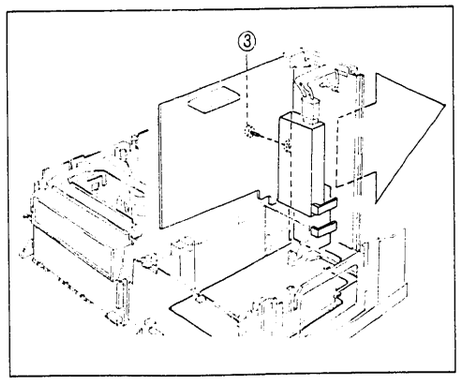


Fig. 5 Rear Panel

6. Remote Controller

1) Semove the screw.
2) Release 8 stoppers.

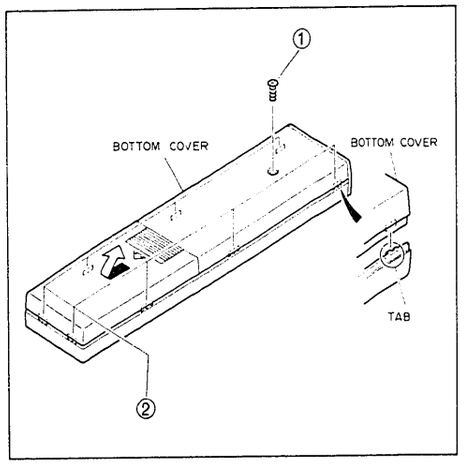


Fig. 6 Remote Controller

4. CIRCUIT BOARD REMOVAL

1. Main Ciarcuit Board
2. Operation Switch Circuit Board
3. Timer Circuit Board
4. Regulator Circuit Board
5. Regulator·TR Circuit Board
6. Preamp Circuit Board
7. Servo/System control Circuit Bourd

1. Main Circuit Board (Fig. 1)

1) Remove the top cover (see item 2 in the section on case removal.)
2) Release the 2 stoppers.
3) Remove the 3 screws.

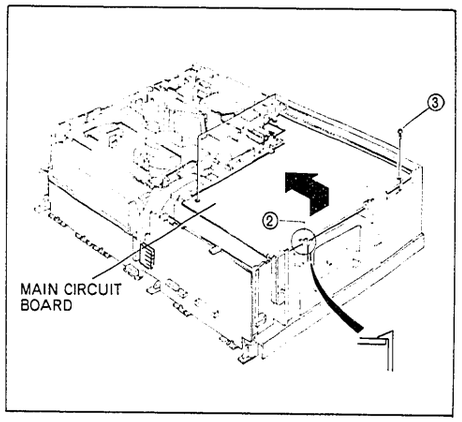


Fig. 1 Main Circuit Board

2. Operation Switch Circuit Board (Fig. 2)

1) Remove the top and bottom covers and the front panel (see items 2, 3 and 4 in the section on case removal.)
2) Disconnect the connector.
3) Release the 6 upper and lower stoppers.

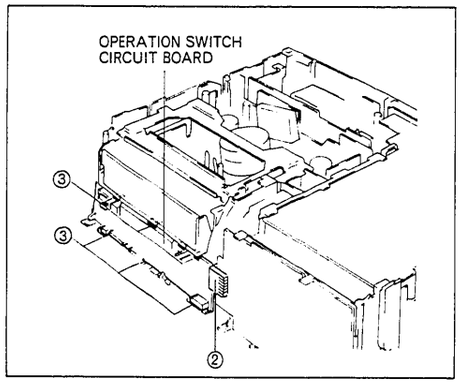


Fig. 2 Operation Switch Circuit Board

3. Timer Circuit Board (Fig. 3)

1) Remove the top and bottom covers and the front panel (see items 2, 3 and 4 in the section on case removal.)
2) Disconnect the connector.
3) Release the 4 upper and lower stoppers.

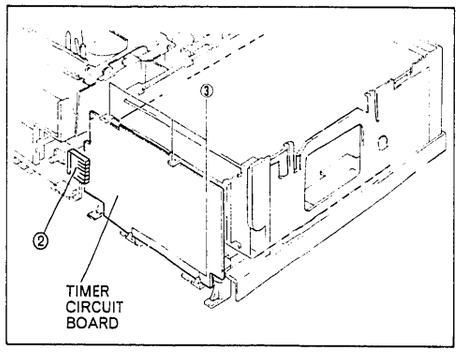


Fig. 3 Timer Circuit Board

4. Regulator Circuit Board (Fig. 4)

1) Remove the top cover (see item 2 in the section on case removal).
2) Remove the screw from the bottom cover.
3) Remove the 2 screws on the transformer holder.
4) Lift up in the direction of the arrow.

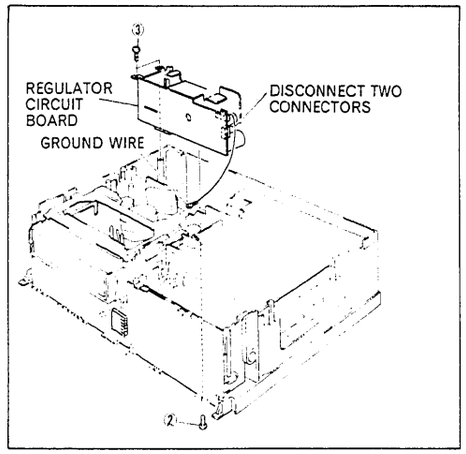


Fig. 4 Regulator Circuit Board

5. Regulator·TR Circuit Board (Fig. 5)

1) Remove the top cover (See item 2 in the section on case removal).
2) Remove the screw holding the circuit board holder.

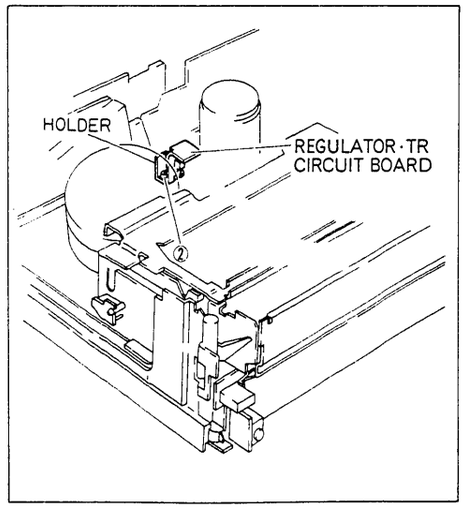


Fig. 5 Regulator·TR Circuit Board

6. Preamp Circuit Board (Fig. 6)

1) Remove the top cover (see item 2 in the section on case removal).
2) Pull out and up.

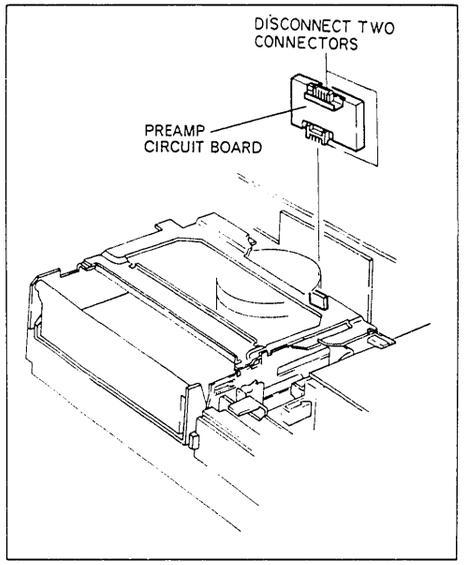


Fig. 6 Preamp Circuit Board

7. Servo/System control Circuit Board (Fig. 7)

1) Remove the bottom cover (See item 3 in the section on case removal).
2) Remove the 2 screws.

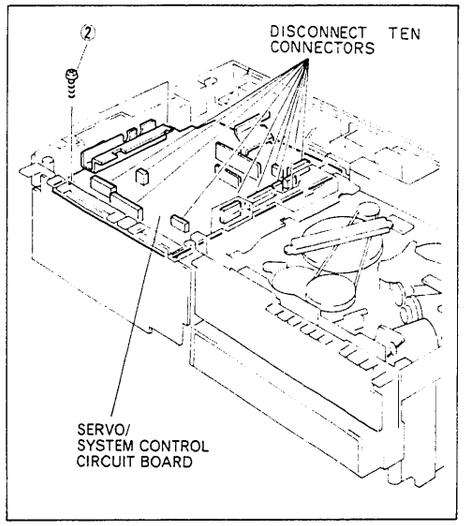


Fig. 7 Servo/System control Circuit Board

5. CASSETTE LOADING MECHANISM REMOVAL

1. **Cassette Door**
2. **Supply End Sensor**
3. **Chassis Holder**

* Components listed below will be described as if the top and bottom covers, front panel have already been removed. (See items 2, 3 and 4 in the section on case removal.)

4. **Cassette Loading Mechanism**
5. **Gear Cover**
6. **Door Arm**
7. **Drive Gear (L)**
8. **Motor Block**
9. **Cassette Loading Motor**
10. **Drive Gear (R)**
11. **Cassette Holder**

1. Cassette Door (Fig. 1)

1) Remove the top and bottom covers and the front panel (see items 2, 3 and 4 in the section on case removal).
2) Push and spread apart the front holder in the direction indicated by the arrow. Remove the cassette door.

[Cautions during reassembly]

* Make sure the pin on the door arm fits into the groove in the cassette door.

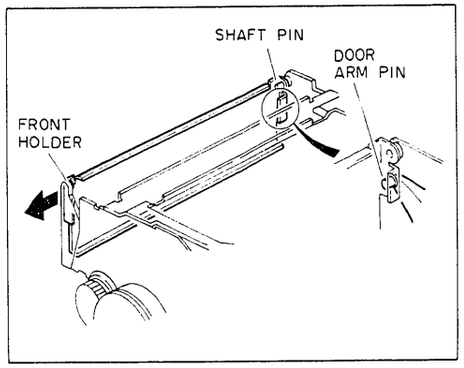


Fig. 1 Cassette Door

2. Supply End Sensor (Fig. 2)

1) Remove the top cover (see item 2 in the section on case removal).
2) Release the stopper.

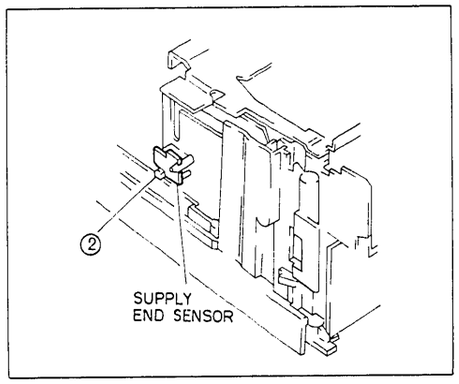


Fig. 2 Supply End Sensor

3. Chassis Holder (Fig. 3)

1) Remove the top cover (see items 2 in the section on case removal).
2) Remove the supply end sensor (see item 2).
3) Release the supply end sensor cord from the chassis holder.
4) Remove the 4 screws.

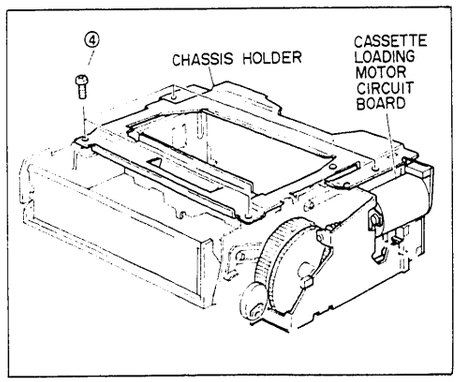


Fig. 3 Chassis Holder

4. Cassette Loading Mechanism (Fig. 4)

1) Remove the top cover and front panel (See items 2 and 4 in the section on case removal).
2) Disconnect the connector.
3) Remove the 2 screws.
4) Lift the rear end of the mechanism upwards and release the engagement fitting on the bottom front.

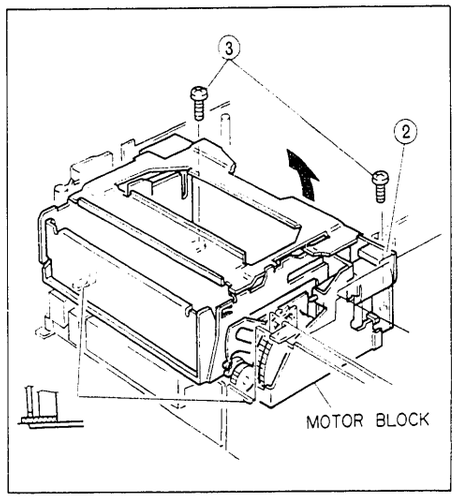


Fig. 4 Cassette Loading Mechanism

5. Gear Cover (Fig. 5)

1) Remove the cassette loading mechanism (see item 4).
2) Lift section (A) up slightly. Then pull the entire gear cover unit forward.

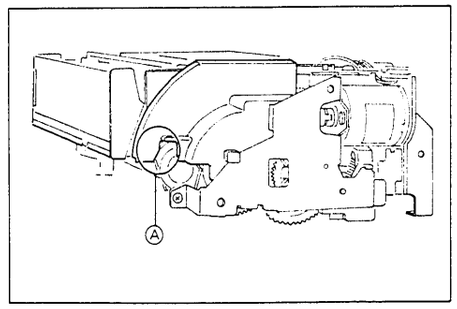


Fig. 5 Gear Cover

6. Door Arm (Fig. 6)

1) Remove the cassette loaidng mechanism (see item 4.)
2) Remove the spring.
3) Release the 2 stoppers.

[Cautions during reassembly]

* Insert the pin on the front edge of the door arm into the groove in the cassette door.

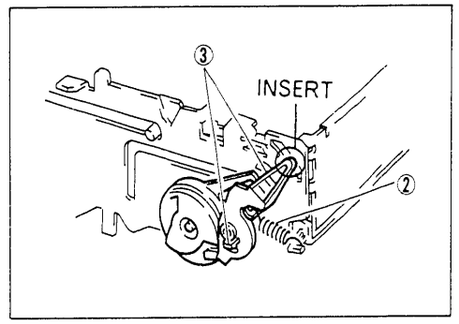


Fig. 6 Door Arm

7. Drive Gear (L) (Fig. 7)

1) Remove the cassette loading mechanism and the door arm (see items 4 and 6).
2) Release the stopper and pull out the drive gear (L).

[Cautions during reassembly]

* Align the triangular mark on the drive gear (L) with the triangular mark on the synchro gear (L).
* Insert the pin on the cassette holder into the groove in the drive arm.

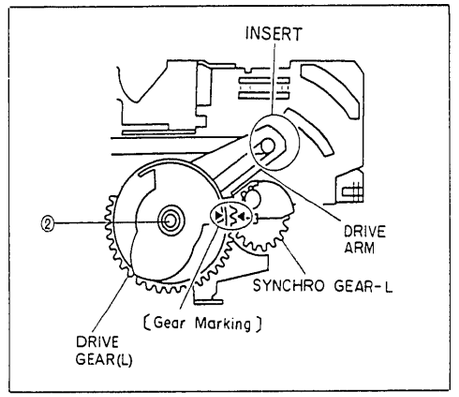


Fig. 7 Drive Gear (L)

8. Motor Block (Fig. 8)

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor and the chassis holder (see items 4, 5, 2 and 3).
2) Remove the 2 screws holding the motor block.

[Cautions during reassembly]

* Place the cassette holder in the unloaded position (prior to cassette insertion). Align the triangular markings on the synchro gear and the clutch gear.
* Insert the slide pin on the cassette holder into the groove in the clutch gear's drive arm.

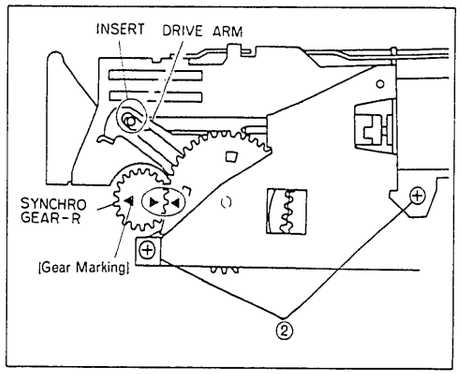


Fig. 8 Cassette Loading Motor Block

9. Cassette Loading Motor (Fig. 9)

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor, the chassis holder and the motor block (see items 4, 5, 2, 3 and 8).
2) Remove the 2 screws holding the cassette loading motor.

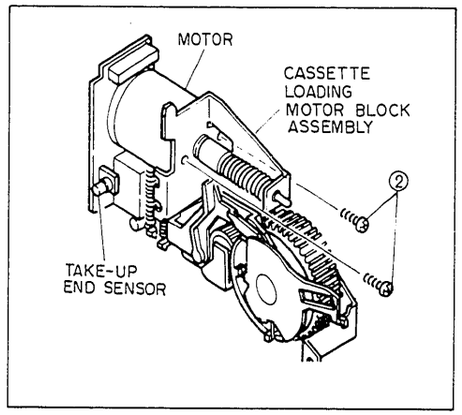


Fig. 9 Cassette Loading Motor

10. Drive Gear (R) (Figs. 10, 11 and 12)

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor, the chassis holder and the motor block (see items 4, 5, 2, 3 and 8).
2) Remove the 2 springs. Pull the switch lever out.
3) Turn the drive arm counterclockwise and pull the clutch gear out.
4) Release the stopper. Pull out another gear.
5) Remove the screw holding the gear holder.

[Cautions during reassembly]

* Position the triangular marking on the drive gear (R) so that it faces the worm gear. (See Fig. 11). The ○ and triangle can also be seen from the outside so that correct position can be checked after reassembling the motor block. (See Fig. 12)
* Align marking (▷) on drive gear (R) with projection (◁) on the clutch gear. (See Fig. 11)
* Attach the spring on the clutch gear to both gears (See Fig. 11)

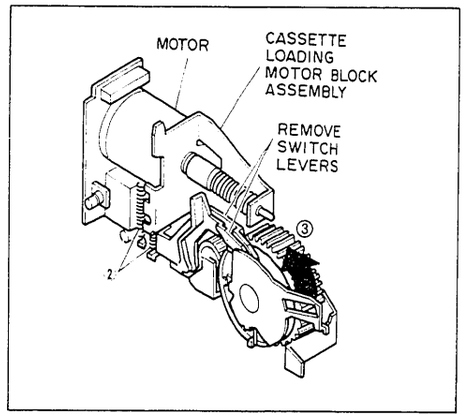


Fig. 10 Drive Gear (I)

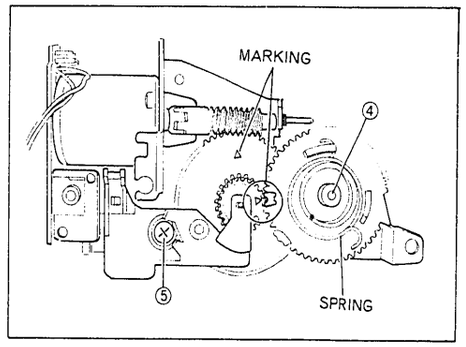


Fig. 11 Drive Gear (II)

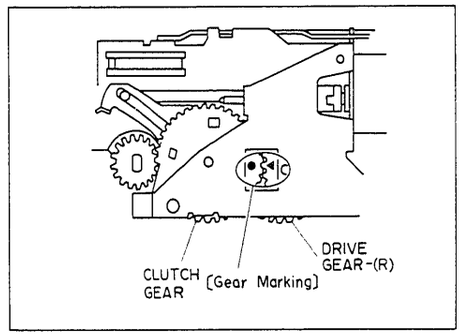


Fig. 12 Marking on Gear

11. Cassette Holder (Fig. 13)

1) Remove the cassette loading mechanism, the gear cover, the supply end sensor, the chassis holder and the motor block (see items 4, 5, 2, 3 and 8).
2) Remove the screw on top of the front holder. Remove the side chassis (R)

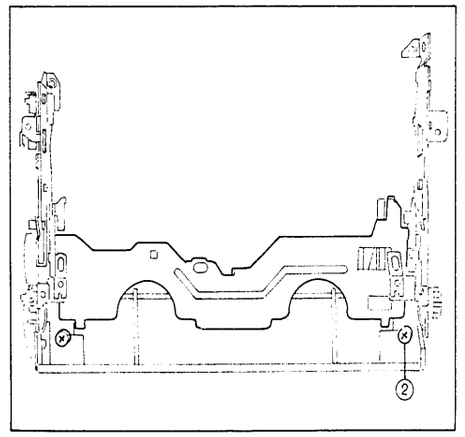


Fig. 13 Cassette Holder

6. MAIN MECHANICAL COMPONENTS REMOVAL

Heads

1. Upper Cylinder (Video Heads)
2. Impedance Roller and FE (Full Erase) Head
3. A/C (Audio Control) Head

Motors

4. Cylinder Assembly
   Rotor Magnet
   FG Coil
5. Capstan Motor
6. Loading Motor

Sensors, Switches

7. End Lamp
8. Reel Sensor
9. Mechanism State Switch
10. Safety Tab Switch

Others

11. Main Brake
12. Supply Subbrake
13. Supply Guide Pole
14. Take-up Guide Pole
15. Reel Drive Gear
16. Take-up Reel Disk
17. Load Pulley
18. Tension Arm/Tension Band
19. Guide Roller
20. Supply Reel Disk
21. Pressure Roller
22. Arm Bracket Bracket
23. Guide Base and Loading Link
24. Clutch Plate Assembly
25. Brake Slider
26. Capstan Flywheel
27. Loading Gear Assembly

1. Upper Cylinder (Video Heads) (Figs. 1 and 2)

1) Remove the top cover (see item 2 in the section on case removal)
2) Remove the screw holding the brush.
3) Remove the 2 screws holding upper cylinder. Pull the upper cylinder out.

[Cautions while working]

* Since the upper cylinder has connectors, do not apply pressure in the direction of rotation. Pull the cylinder vertically upward in the direction of cylinder attachment.
* Do not touch the video head tips with fingers or tools.

[Cautions during reassembly]

* Insert so that the arrow on the rotary transformer matches the blue side of the video head connector.
* Alternately tighten the 2 screws holding the upper cylinder.

[Adjustments after reassembly]

○ Adjustments after replacing the cylinder

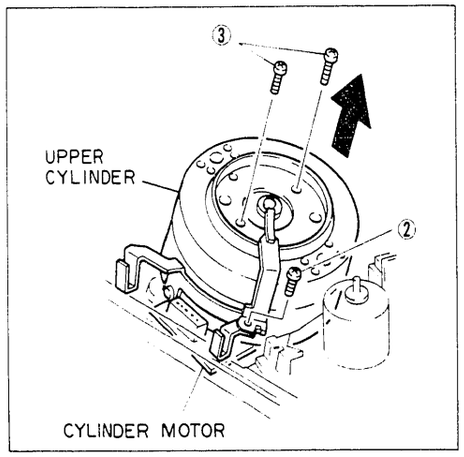


Fig. 1 Video Head

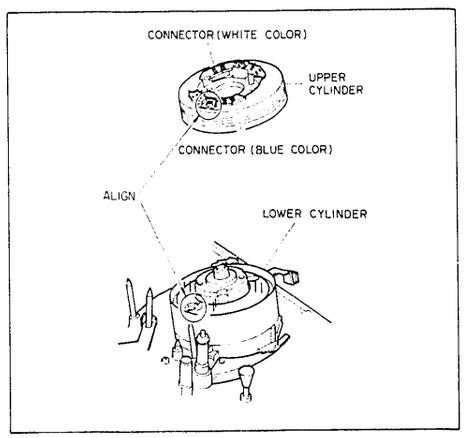


Fig. 2 Rotary Transformer

2. Impedance Roller and FE (Full Erase) Head (Fig. 3)

1) Remove top cover (see item 2 in the section on case removal).
2) Disconnect the connector.
3) Remove the spring attached between the FE head base and the chassis.
4) Remove the lock nut on the guide pole and then pull the guide pole, spring and washer out.
5) Pull up the FE head together with the base and out.
6) Then with the FE head removed, remove the screw on the back of the base.

[Adjustments after reassembly]

○ Guide pole height adjustment

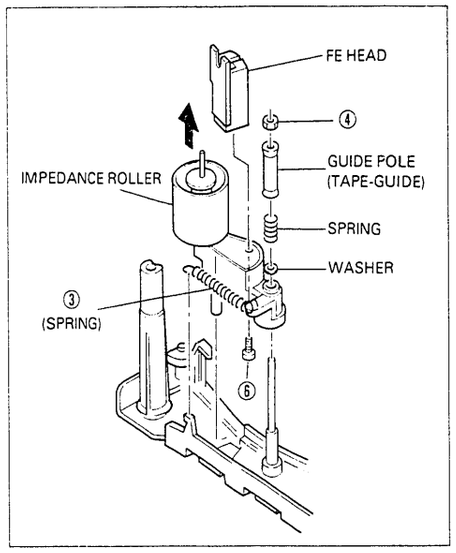


Fig. 3 FE Head

3. A/C (Audio/Control) Head (Figs. 4 and 5)

1) Remove the top cover (see item 2 in the section on case removal).
2) Pull out the connector.
3) Remove the lock nut and washer from the head base. Pull up the base and out.

* Apply the bottom of the spring under the head base to the stopper on the chassis, the top of the spring to the stopper on the base. (Fig. 6)

[Cautions during reassembly]

* Make sure the tip of the A/C head base screw protrudes 3 to 4 mm from the top surface of head base 1.
* Make sure that head base 1 and head base 2 are parallel.

[Adjustments after reassembly]

○ A/C head adjustment
○ X value adjustment
○ Audio playback level adjustment
○ Audio bias level adjustment

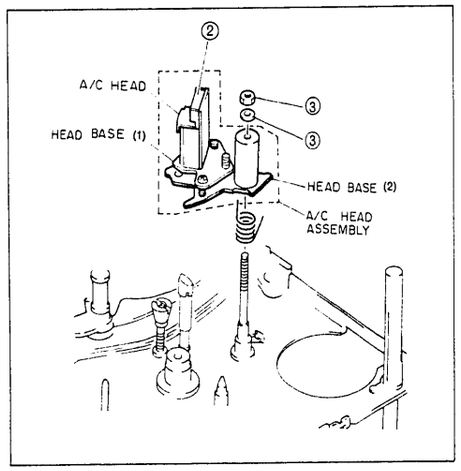


Fig. 4 AC Head

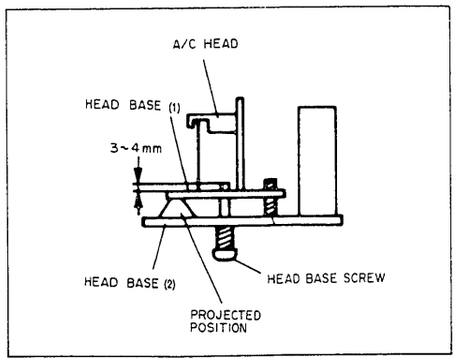


Fig. 5 Spring and Lock Screw

4. Cylinder Assembly (Figs. 6 and 7)

1) Remove the top cover (see item 2 in the section on case removal).
2) Pull out the preamp circuit board.
3) Remove the bottom cover (see item 3 in the section on case removal.)
4) Disconnect the connector from the FG circuit board.
5) Remove the 3 screws holding the cylinder.
6) Remove the cylinder assembly from the top.

[Cautions during reassembly]

* Since the screws position on the back of the assembly, place the unit with the left side down to remove the screws.
* Do not touch the video head tips with fingers or tools.

[Adjustments after reassembly]

○ Adjustments after replacing the cylinder

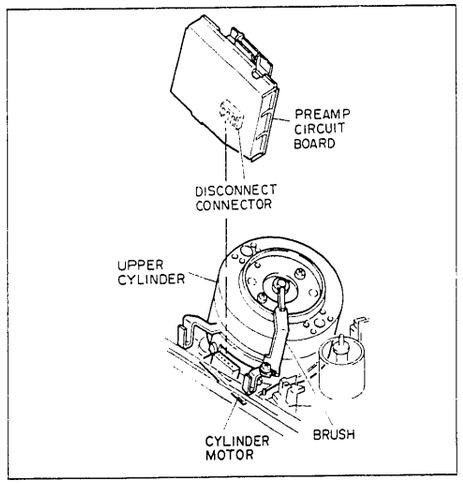


Fig. 6 Cylinder Assembly —Top View—

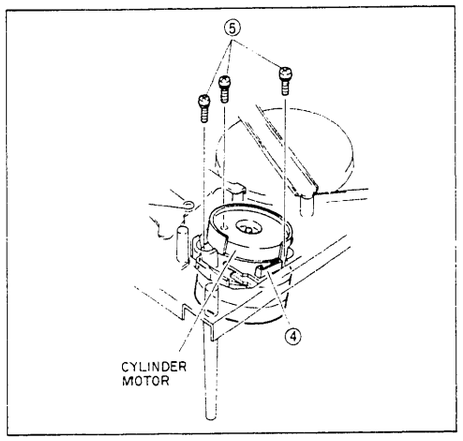


Fig. 7 Cylinder Assembly —Bottom View—

[Removing only the rotor magnet and FG coil]
(Figs. 8 and 9)

1) Remove the bottom cover (see item 3 in the section on case removal).
2) Remove the 2 screws on the rotor. Pull the rotor magnet out.
3) Remove the 3 screws holding the FG coil.

[Cautions during reassembly]

* Fit the slot on the cylinder rotating spindle into the protrusion on the rotor side, then lock the rotor magnet with the screws.

[Adjustments after reassembly]

○ Switching point adjustment

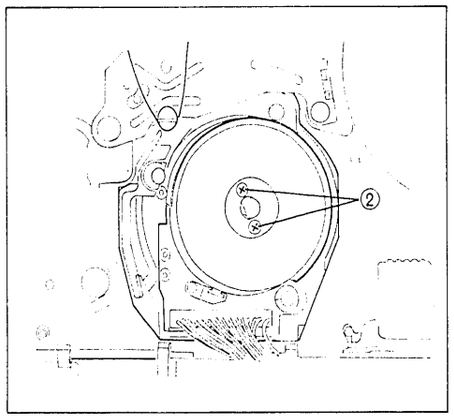


Fig. 8 Rotor Magnet

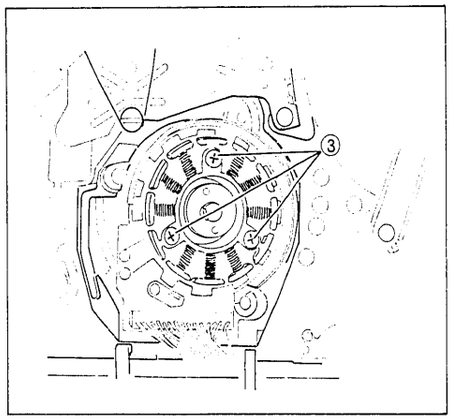


Fig. 9 FG Coil

5. Capstan Motor (Fig. 10)

1) Remove bottom cover (see item 3 in the section on case removal).
2) Remove the reel belt.
3) Remove the flywheel belt.
4) Disconnect the connector from the capstan motor circuit board.
5) Remove the 2 screws holding the capstan motor holder. Pull out the capstan motor holder.

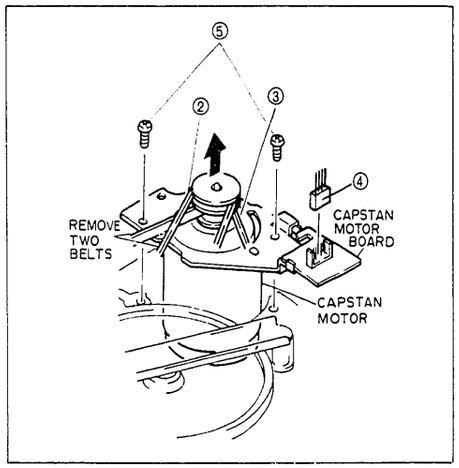


Fig. 10 Capstan Motor

6. Loading Motor (Fig. 11)

1) Remove the bottom cover (see item 3 in the section on case removal.)
2) Remove the loading belt.
3) Disconnect the connector from the loading motor circuit board.
4) Remove the screw holding the loading motor.

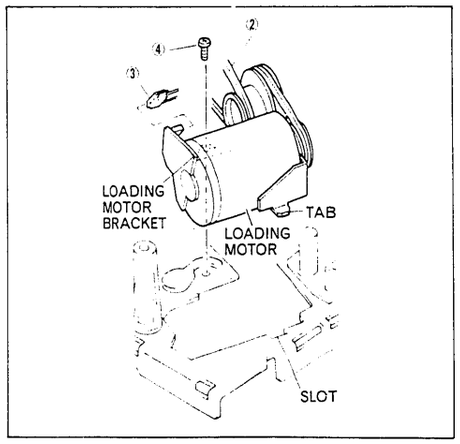


Fig. 11 Loading Motor

7. End Lamp (Fig. 12)

1) Remove the top cover (see item 2 in the section on case removal).
2) Remove the screw holding the end lamp.

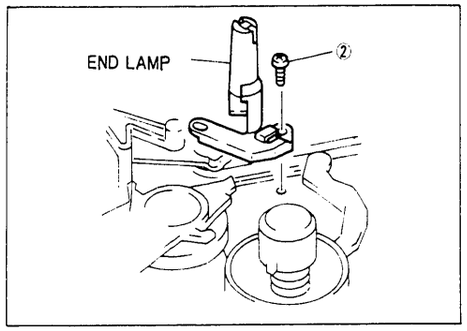


Fig. 12 End Lamp

8. Reel Sensor (Fig. 13)

1) Remove the bottom cover (see item 3 in the section on case removal).
2) Remove the screw holding the reel sensor.

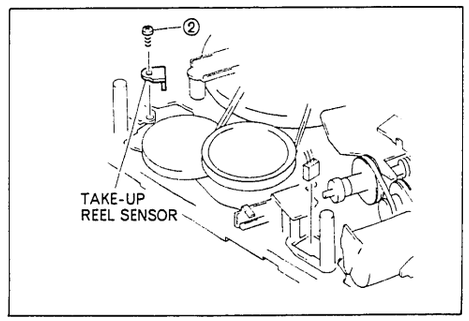


Fig. 13 Reel Sensor

9. Mechanism State Switch (Fig. 14)

1) Remove the bottom cover (see item 3 in the section on case removal).
2) Disconnect the connector.
3) Remove the screw holding the mechanism state switch.

[Adjustments after reassembly]

○ Mechanism state switch adjustment

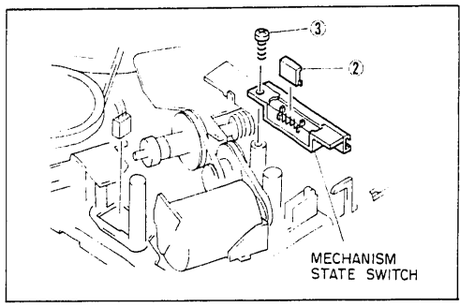


Fig. 14 Mechanism State Switch

10. Safety Tab Switch (Fig. 15)

1) Remove the top and bottom covers (see items 2 and 3 in the section on case removal).
2) Disconnect the connector from the bottom side.
3) Remove the screw holding the safety tab switch.

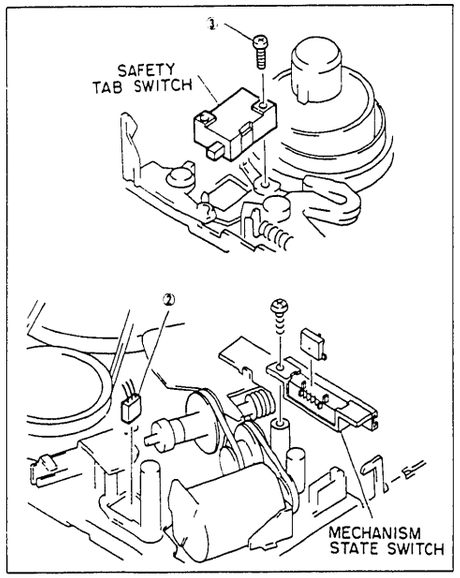


Fig. 15 Safety Tab Switch

* Components in items 11 to 17 are described as if the top cover has already been removed. See item 2 in the section on case removal.

11. Main Brakes (Fig. 16)

1) Remove the springs between the supply and take-up brakes.
2) Release each section engaged with the chassis.

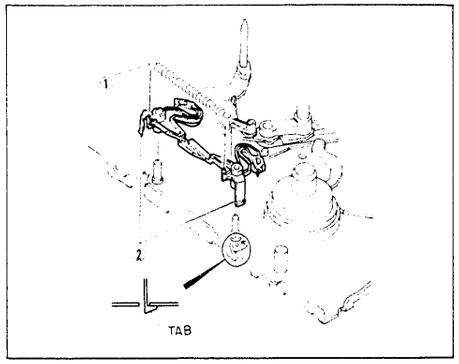


Fig. 16 Main Brakes

12. Supply Subbrake (Fig. 17)

1) Remove the spring between the subchassis and the brake.
2) Release the section engaging the brake spindle.

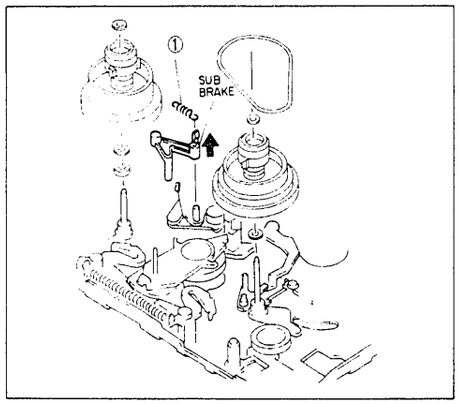


Fig. 17 Supply Subbrake

13. Supply Guide Pole (Fig. 18)

1) Remove the screw holding the guide pole.

[Cautions during reassembly]

* Make sure the washer and spring are inserted in the guide pole attachment shaft.

[Adjustments after reassembly]

○ Guide pole height adjustment

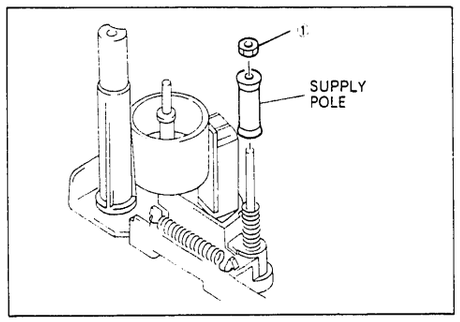


Fig. 18 Supply Guide Pole

14. Take-up Guide Pole (Fig. 19)

1) Remove the cap. Remove the screw holding the guide pole.

[Cautions during reassembly]

* Make sure the spring is inserted in the guide pole attachement shaft.

[Adjustments after reassembly]

○ Guide pole height adjustment

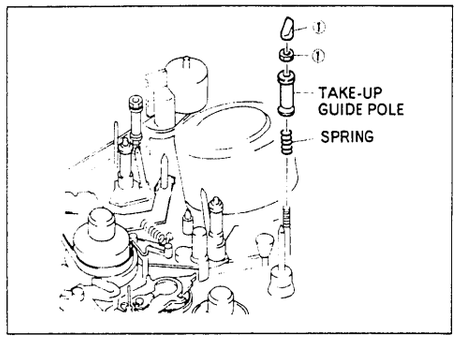


Fig. 19 Take-up Guide Pole

15. Reel Drive Gear (Fig. 20)

1) Push the spring holder in the direction of arrow to pull the spring holder up and out.

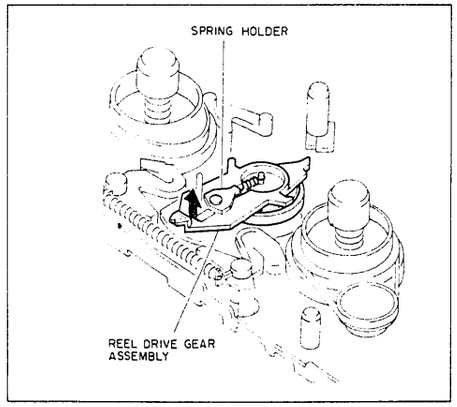


Fig. 20 Reel Drive Gear

16. Take-up Reel Disk (Fig. 21)

1) Remove the rubber belt across the load pulley and reel disk.
2) Remove the washer from the top of the disk.

[Cautions during reassembly]

* Make sure the washer is inserted in the reel disk attachment shaft.

[Adjustments after reassembly]

○ Reel disk height adjustment

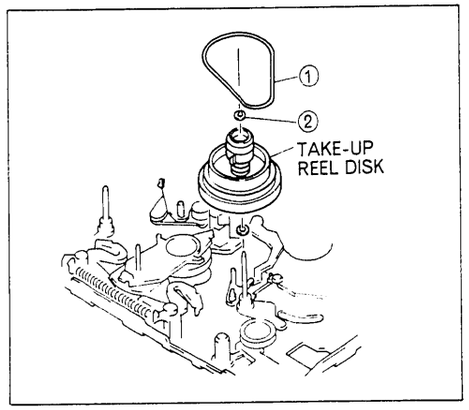


Fig. 21 Take-up Reel Disk

17. Load Pulley (Fig. 22)

1) Remove the rubber belt across the pulley and the reel disk.
2) Remove the washer from the top of the pulley.

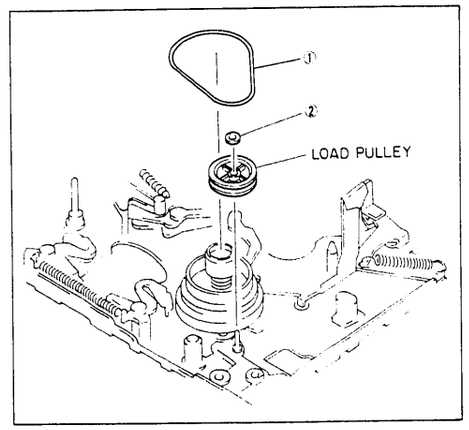


Fig. 22 Load Pulley

* Components in items 18 to 23 are described as if the top and bottom covers, the front panel and cassette loading mechanism have already been removed. See item 4 in the section on cassette loading mechanism removal and items 2, 3 and 4 in the section on case removal.

18. Tension Arm/tension Band (Fig. 23)

1) Remove the spring across the tension arm and spring holder.
2) Remove the screw holding the tension band.
3) Release the engagement section with the tension arm. Pull out the tension arm and tension band.

[Adjustments after reassembly]

○ Adjustments of tension and tension pole position.

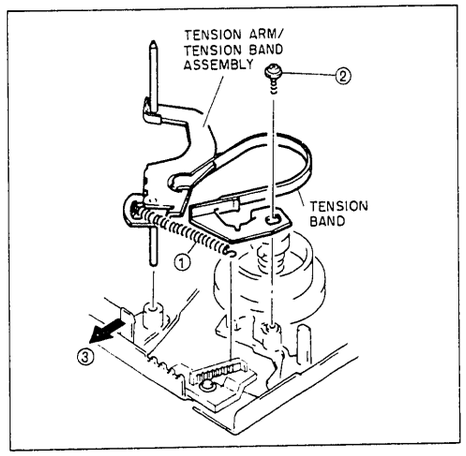


Fig. 23 Tension Arm tension Band

19. Guide Roller (Fig. 24)

* Remove the supply and take-up sides in the same way.

1) Loosen the hex lock nut on the guide roller.
2) Turn the guide roller counterclockwise to remove.

[Adjustments after reassembly]

○ Guide roller height adjustment

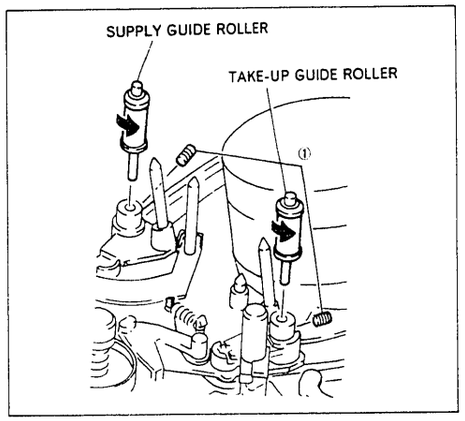


Fig. 24 Guide Roller

20. Supply Reel Disk (Fig. 25)

1) Remove the supply subbrake and tension arm/tension band (see items 12 and 18).
2) Remove the washer from the top of the disk.

[Cautions during reassembly]

* Make sure the washer and collar are inserted in the reel disk attachment shaft.

[Adjustments after reassembly]

○ Adjustments of tension and tension pole position.
○ Reel disk height adjustment

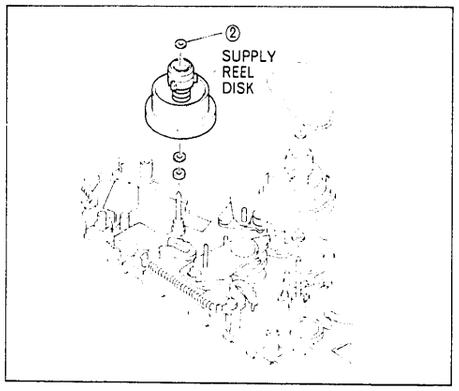


Fig. 25 Supply Reel Disk

21. Pressure Roller (Fig. 26)

1) Remove washer.

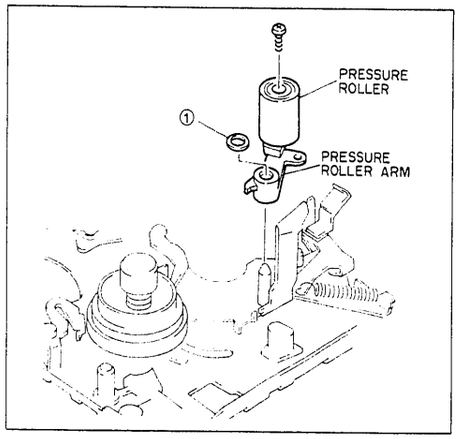


Fig. 26 Pressure Roller

22. Arm Bracket Assembly (Fig. 27)

1) Remove the take-up reel disk and pressure roller (see items 16 and 21).
2) Release the 2 cords from the chassis.
3) Remove the 2 screws. Pull out the arm bracket assembly.

[Cautions during reassembly]

* Insert operation arm spindle into slot in take-up brake operation arm.
* Insert drive arm spindle into slot in link piece.

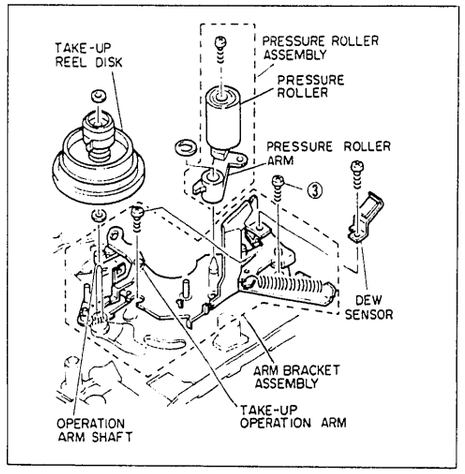


Fig. 27 Arm Bracket Assembly

23. Guide Base/Loading Link (Fig. 28)

1) Remove supply subbrake and tension band/tension arm. (See items 12 and 18)
2) Remove the 3 screws holding the subchassis. Remove the subchassis and guide base.

[Cautions during reassembly]

* When reinstaling the loading link, make sure that the projection on the loading gear is aligned with the groove in the loading link.
* When reinstalling the guide base, make sure that the pin on the back of the guide base is inserted into the slot in the loading link.

[Adjustments after reassembly]

○ Adjustments of tension and tension pole position.

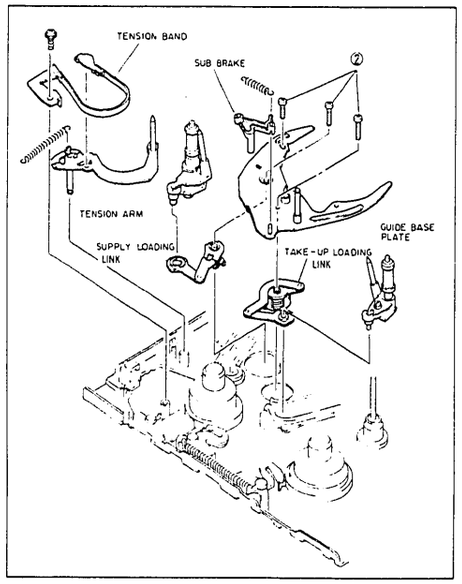


Fig. 28 Guide Base/Loading Link

* Components in items 24 to 26 are described as if the top and bottom covers have already been removed. (See items 2 and 3 in the section on case removal

24. Clutch Plate Assembly (Fig. 29)

1) Remove the reel drive gear (see item 15).
2) Remove reel belt.
3) Remove the 2 screws holding the clutch plate assembly.

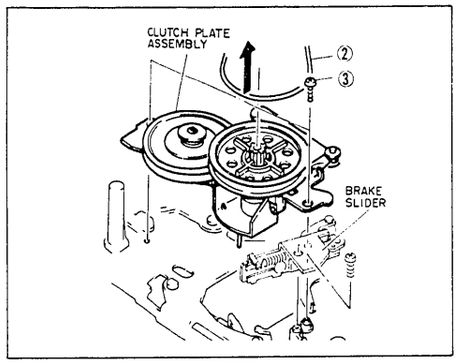


Fig. 29 Clutch Plate Assembly

25. Brake Slider (Fig. 30)

1) Remove the reel drive gear and clutch plate assembly (see items 15 and 24).
2) Remove the screw holding the brake slider.

[Cautions during reassembly]

* Make sure the pin on the brake drive arm is inserted into the groove on the slider operating section.

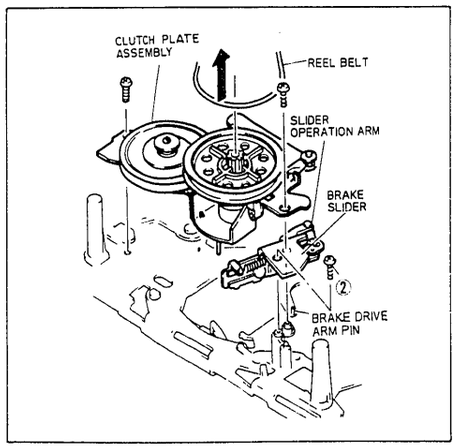


Fig. 30 Brake Slider

26. Capstan Flywheel (Fig. 31)

1) Remove the 2 screws holding the flywheel retainer bar. Remove the flywheel retainer bar.
2) Remove the nylon washer from the top of the capstan shaft.
3) Remove the reel belt and flywheel belt. Remove the flywheel.

[Cautions during reassembly]

* Make sure the washer is inserted between the bottom side of the chassis and the flywheel.

[Adjustments after reassembly]

○ Reference oscillation frequency adjustment

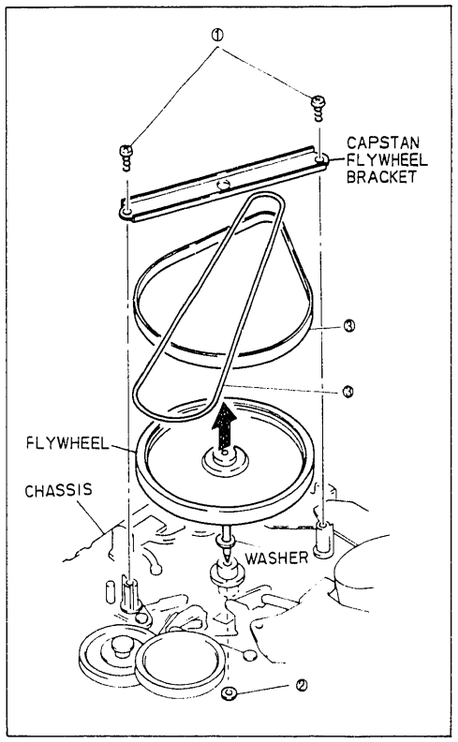


Fig. 31 Capstan Flywheel

27. Loading Gear Assembly (Fig. 32)

1) Remove the top and bottom covers (see items 2 and 3 in the section on case removal).

Top Side

2) Remove the 2 screws from the top of the subchassis.
3) Remove the reel drive gear. (See item 15)

Bottom Side

4) Remove the mechanism state switch, clutch plate assembly, brake slider and capstan flywheel. (See items 9, 24, 25 and 26.)
5) Remove the spring and switch slider from the loading gear assembly.
6) Remove tension release arm.
7) Remove loading belt.
8) Remove the 3 screws holding the loading gear assembly.

[Cautions during reassembly]

* Insert the pin on the take-up subbrake drive arm into the slot on the take-up subbrake operation arm.
* Insert the pin on the pressure roller drive arm into the slot on the pressure roller operation arm.

[Adjustments after reassembly]

○ Mechanism state switch adjustment

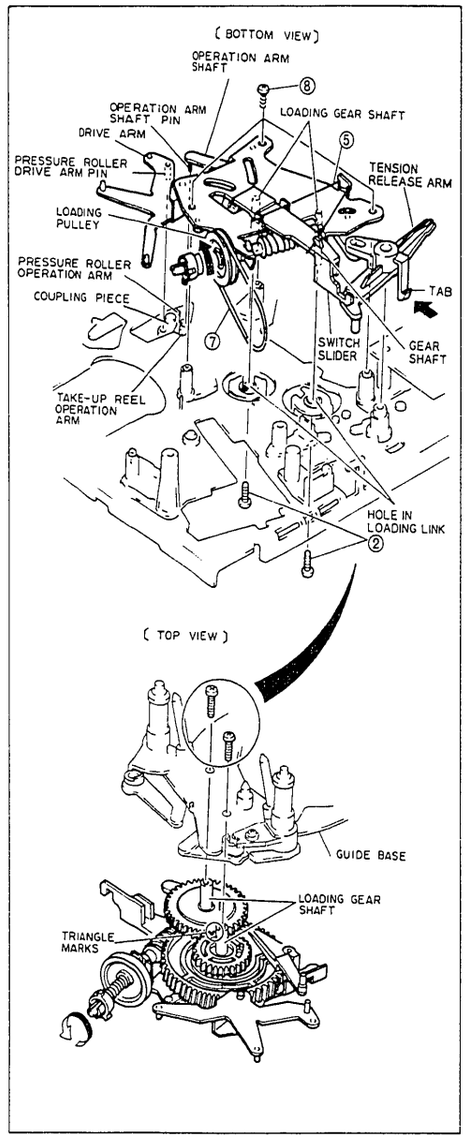


Fig. 32 Loading Gear Assembly (with items in 9, 24, 25 and 26 removed)

CHAPTER 3

ELECTRIC CIRCUIT ADJUSTMENT

Test equipment and tapes necessary for adjustment.

1) Oscilloscope
2) Color bar generator
3) VTVM
4) Frequency counter
5) Monitor TV
6) NTSC alignment tape
7) 30HM P-2 alignment tape
8) Blank tape

Cautions an adjustments

1) If there are no special instructions, the following conditions apply:
   - O Oscilloscope probe: 10 : 1
   - O Oscilloscope synchronization: Auto-sync
   - O Test equipment ground: TP602
   - O Tracking control: center click.
2) When making more than one adjustment, make those adjustments in the order listed.

Resetting microprocessors

All microprocessors installed in the unit will reset once the AC power cord is removed from the wall socket.

Adjust the system/servo circuit board with left side down as shown in Fig. 1.

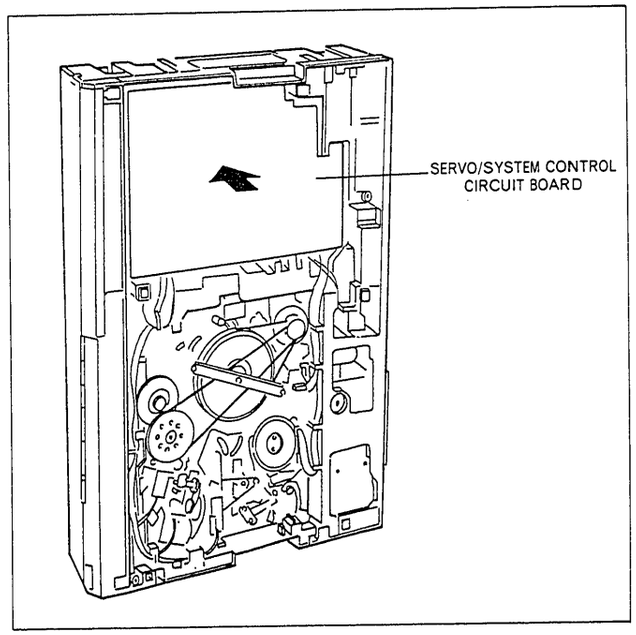


Fig. 1 Ready to Adjust Servo/System control Circuit Board

Place the unit in the horizontal position as shown in Fig. 2 and adjust the main circuit board

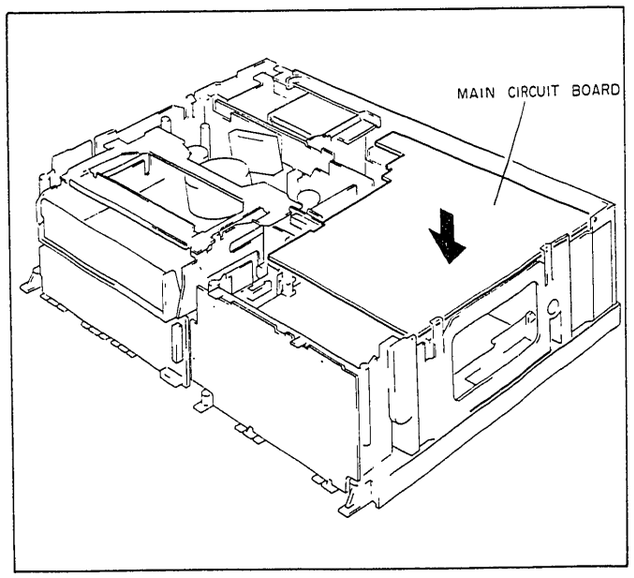


Fig. 2 Ready to Adjust Main Circuit Board

COMPONENTS LOCATIONS ON CIRCUIT BOARDS

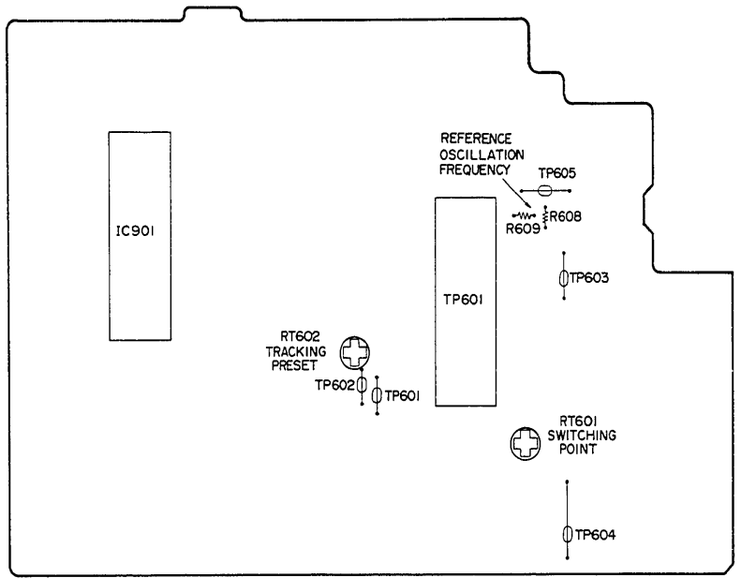


Fig. 3 Components on Servo/System Control Circuit Board (Component Side)

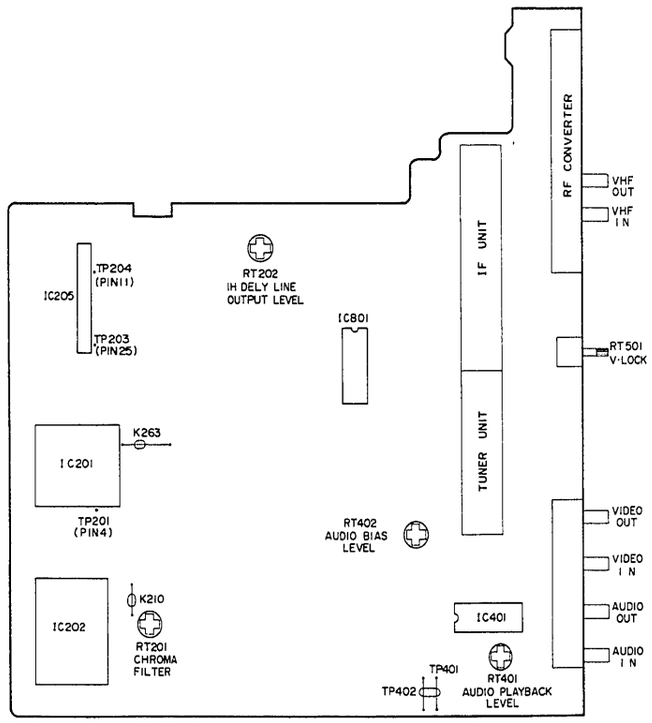


Fig. 4 Components on Main Circuit Board (Soldered Side)

1. SERVO CIRCUIT ADJUSTMENTS

1. Reference Oscillation Frequency Adjustment

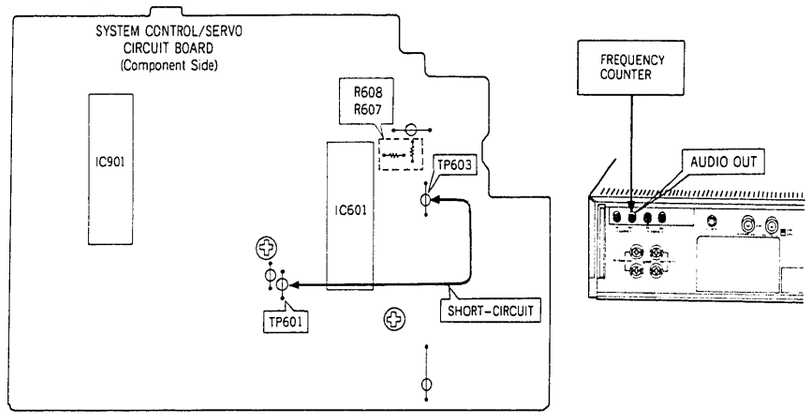
Purpose of adjustment and fault occurring if incomplete

Purpose: Fine tune the reference oscillation frequency (REF30 Hz) in the phase control loop to correct variations in diameters of flywheel, pulley, etc.

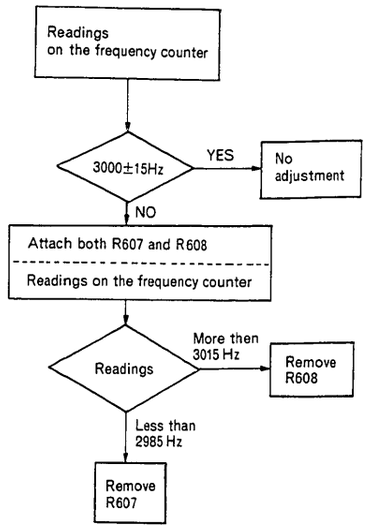
Fault: ○ Noise appears in picture.
○ Tracking cannot be optimized.

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Points
● Frequency counter ● NTSC alignment tape	● Audio output jack	1) Tape speed select switch: SP 2) Alignment tape: Play back 3 kHz portion	● R607 (4.7K) ● R608 (3.9K)

Connections Diagram



Adjustment Procedure



Note: There are some units in which R608 or R609 is removed when shipped from the factory.

2. Switching Point Adjustment

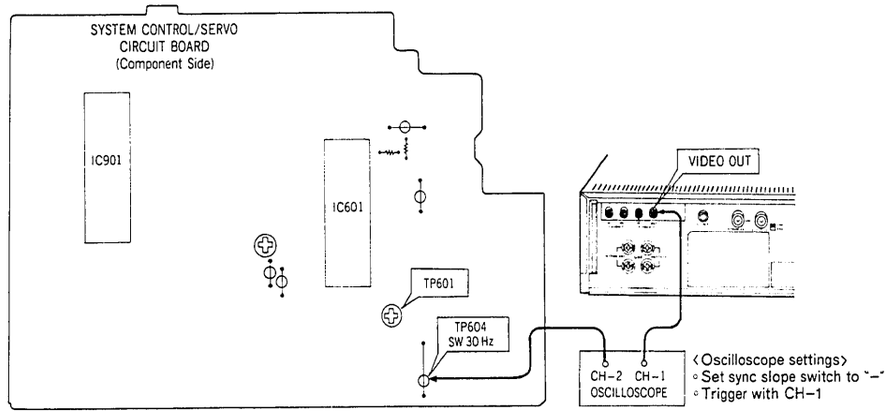
Purpose of adjustment and fault occurring if incomplete

Purpose: Set the video head switching point to almost center where the CH-1 and CH-2 envelopes overlap each other during playback.

Fault: ○ The vertical sync signal is degraded and vertical jitter occurs.
○ Switching noise occurs in lower part of picture.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Oscilloscope ● NTSC alignment tape	● CH-1: video output jack ● CH-2: TP604	● Play back alignment tape	● RT601

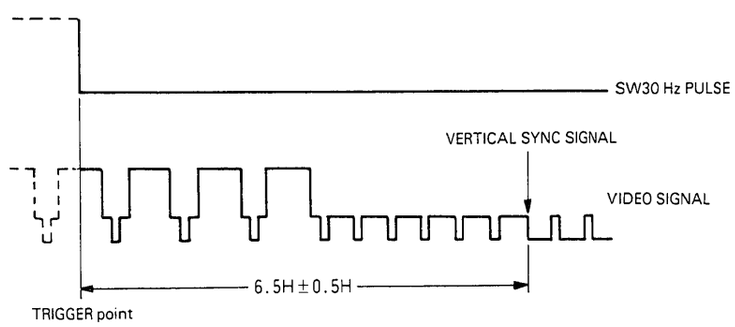
Connections Diagram



Adjustment Procedure

Vertical sync signal:
6.5H ±0.5H from trailing edge (trigger point) of SW30 Hz pulse.

Waveform

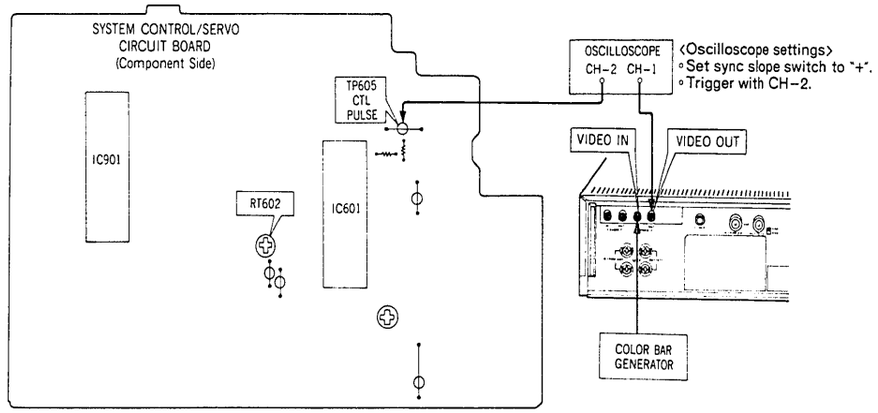


3. Tracking Preset Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Optimize tracking when playing back a tape recorded by this unit.
Fault: ○ Noise occurs even with tracking control centered.
○ Noise cannot be removed by turning the tracking control.

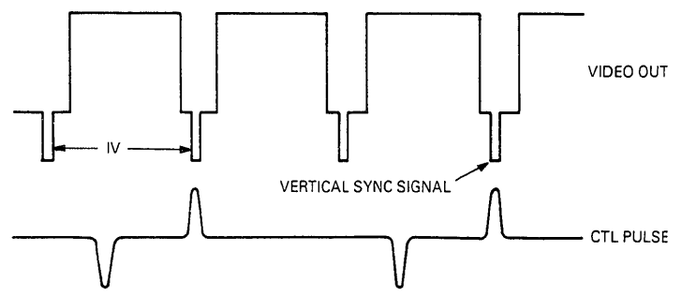
Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Oscilloscope ● Color bar generator (or receive TV program) ● Blank tape	● CH-1: video output jack ● CH-2: TP605	● Record color bar signal in SP mode and play it back with this unit.	● RT602

Connection Diagram



Adjustment Procedure
1) Tracking control: centerd
2) Match phases of CTL pulse (positive pulse) and vertical sync signal

Waveform

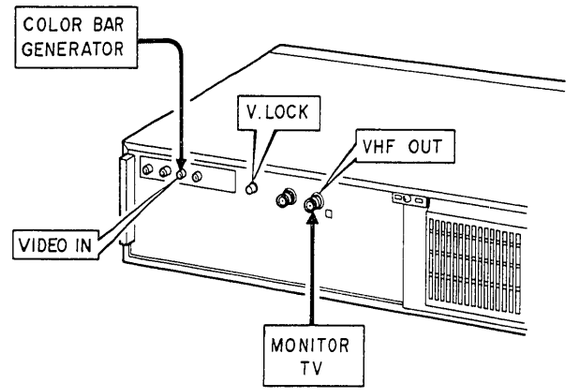


4. V Lock Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Change timing for adding vertical drive pulse and suppress vertical jitter in picture during trick play.
Fault: Vertical jitter during trick play.

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Monitor TV ● Color bar generator (or receive TV program) ● Blank tape	● Check with monitor TV	● Record color bar signal in EP mode and play it back with this unit in still mode.	● RT501

Connection Diagram (Can be adjusted without removing any covers)



Adjustment Procedure
Suppress vertical jitter in picture.

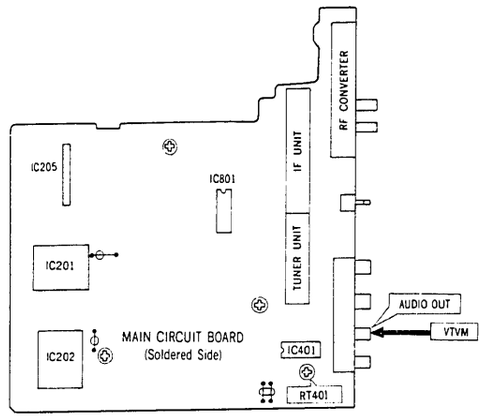
2. AUDIO CIRCUIT ADJUSTMENTS

1. Audio Playback Level Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Set the audio playback level to the specified value.
Fault:

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● VTVM ● NTSC alignment tape	● Audio output jack	● Play back alignment tape	● RT401

Connection Diagram



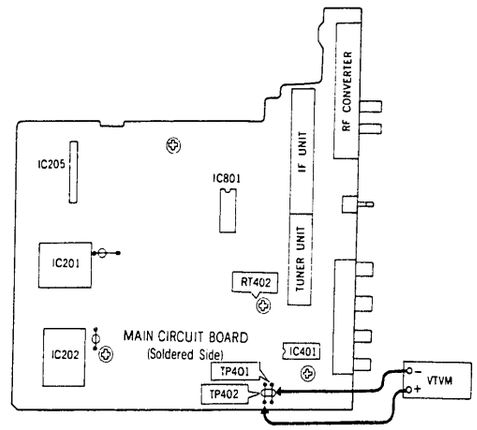
Adjustment Procedure
The VTVM reads −7.8 dBm ± 0.1mVrms.

2. Audio Bias Level Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Set audio bias during recording to optimum level.
Fault: ○ Bias too deep: High-frequency response deteriorates.
○ Bias too shallow: Sound tends to be distorted.

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● VTVM ● Blank tape	● TP401 (−) ● TP402 (+)	● Non-signal recording (SP mode)	● RT402

Connection Diagram



Adjustment Procedure
The VTVM reads 2.4 mV ± 0.1 mVrms.

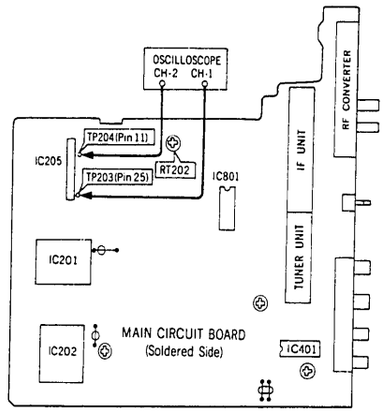
3. LUMINANCE/CHROMA CIRCUIT ADJUSTMENTS

1. 1H Delay Line Output Level Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Makes the input and output levels of the CCD 1H delay line the same.
Fault: Switching noise is conspicuous when dropout is compensated.

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Oscilloscope ● NTSC alignment tape	● TP203(IC205 pin 25) ● TP204(IC205 pin 11)	● Play back color bar signal position of alignment tape	● RT202

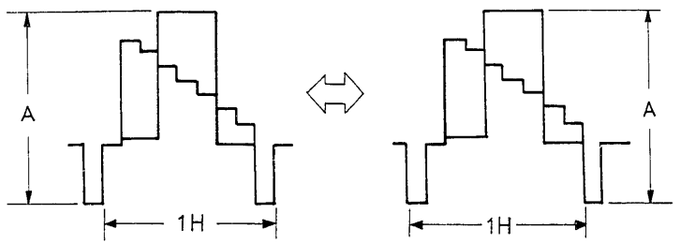
Connection Diagram



Adjustment Procedure
Equalize the CH-1 and CH-2 output levels.

Note : Use the CH-1 level as a reference.

Waveform

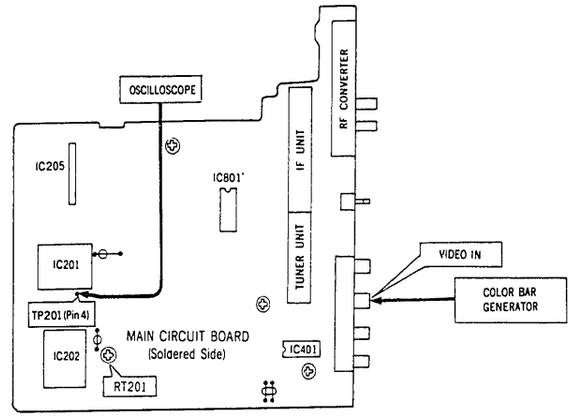


2. Chroma Filter Adjustment

Purpose of adjustment and fault occurring if incomplete
Purpose: Adjust input level of chroma signal subtractor to separate luminance compontents from video signal.
Fault: The luminance S/N deteriorates.

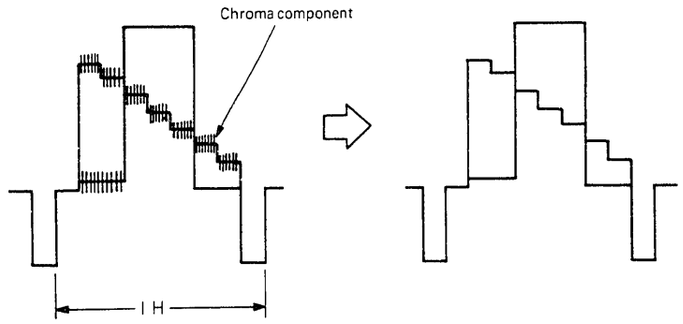
Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Oscilloscope ● Color bar generator	● TP201(IC201 pin 4)	● E-E mode	● RT201

Connection Diagram



Adjustment Procedure
Minimize chroma component

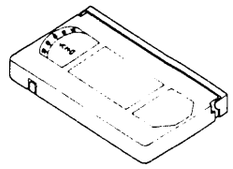
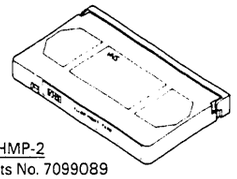
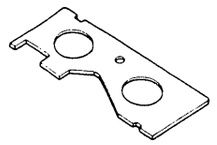
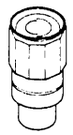
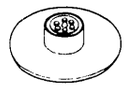
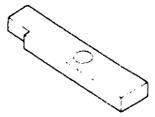
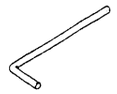
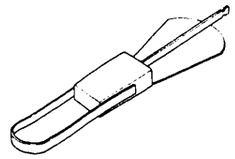
Waveform



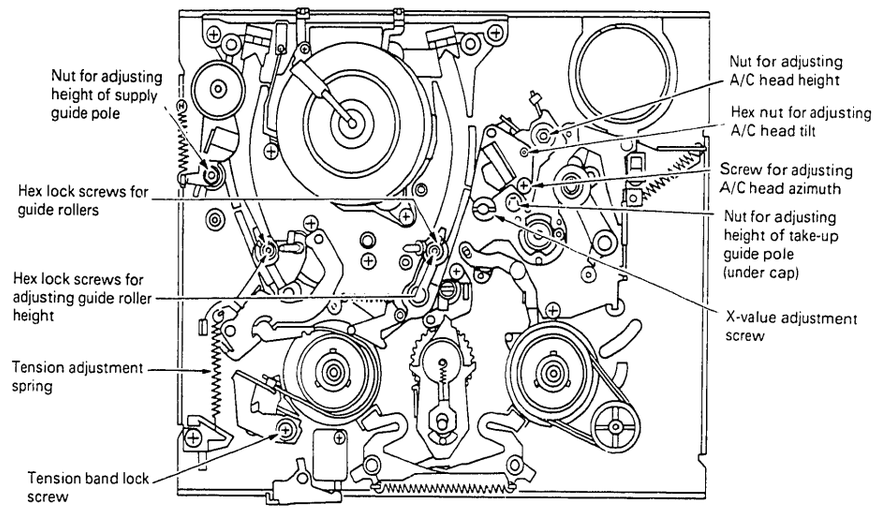
CHAPTER 4

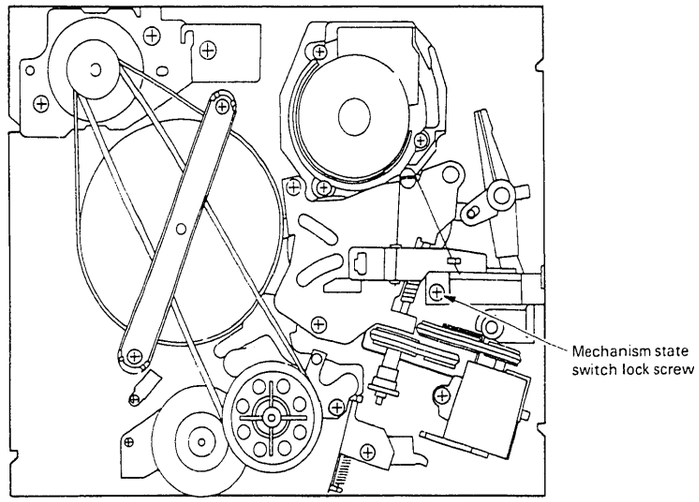
MECHANISM ADJUSTMENT

SERVICING JIGS AND TOOLS

1. Back tension meter Parts No. 7099004 	2. NTSC alignment tape Parts No. 7099052  30HMP-2 Parts No. 7099089	3. Height reference plate (master plane) Parts No. 7099041 
4. Torque gauge Parts No. 7099039 	5. Torque gauge adapter Parts No. 7099035 	6. Dummy reel Parts No. 7099043 
7. Reel disk height jig Parts No. 7099038 	8. 1.5 mm hexagonal wrench 	9. Fan-shaped tension gauge 

LIST OF ADJUSTMENT LOCATIONS


Nut for adjusting height of supply guide pole
Hex lock screws for guide rollers
Hex lock screws for adjusting guide roller height
Tension adjustment spring
Tension band lock screw
Nut for adjusting A/C head height
Hex nut for adjusting A/C head tilt
Screw for adjusting A/C head azimuth
Nut for adjusting height of take-up guide pole (under cap)
X-value adjustment screw



MECHANICAL COMPONENT ADJUSTMENT

1. Mechanism State Switch Adjustment

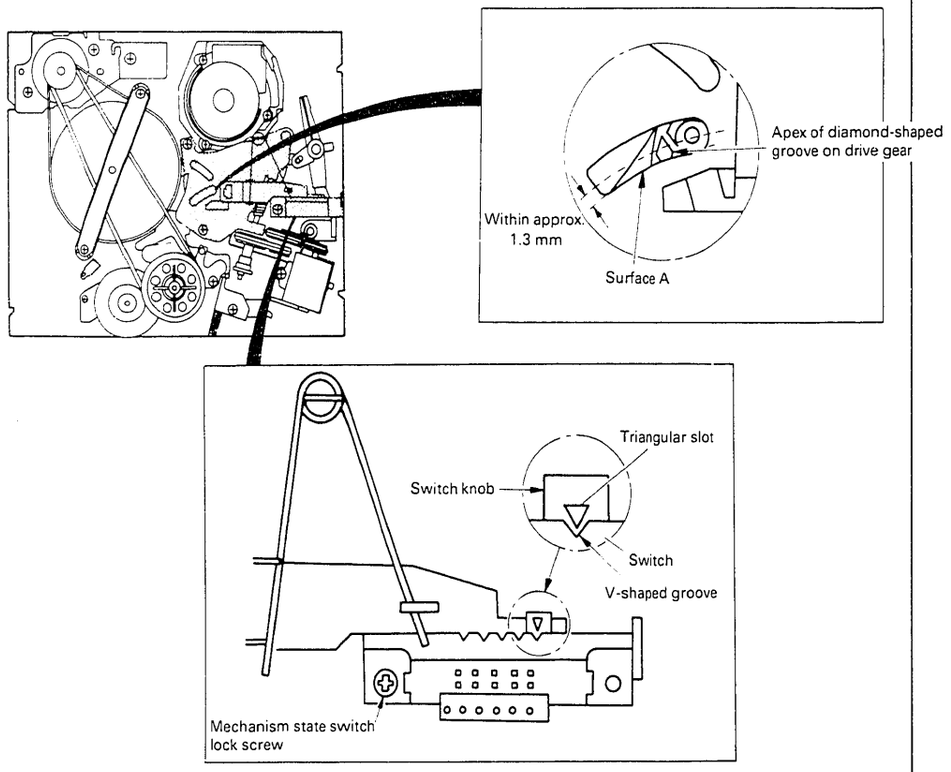
Purpose: Accurately detect mechanism states and prevent malfunction.

Test Equipment/Jigs	VTR State	Adjustment Point
● Blank tape	● Stop mode	● Mechanism state switch lock screw

Adjustment Procedure

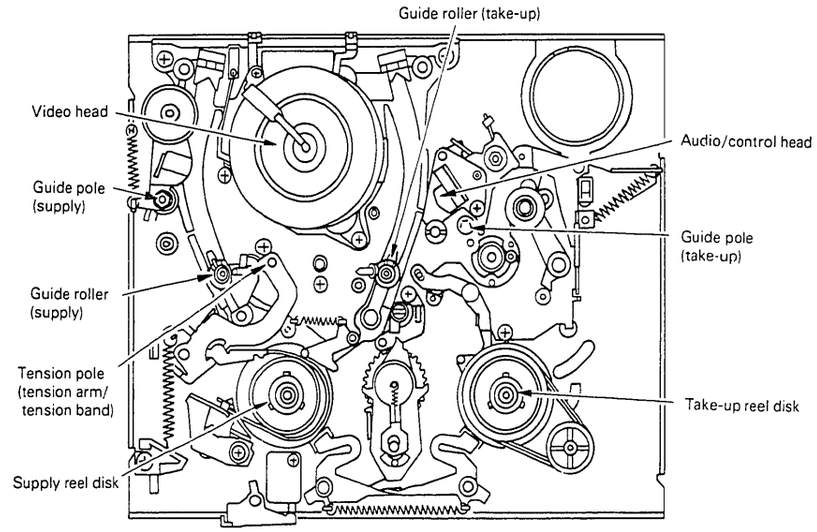
1) Turn the worm pulley by hand. Position the apex of the diamond-shaped groove on the drive gear so that it is within 1.3 mm from the A surface of the gear plate.
2) Loosen the lock screw on the mechanism state switch. Slide the switch so that the apex of the triangular slot on the switch knob is aligned with the V-shaped groove on the extreme outside of the switch.
3) Loosen the lock screw. Insert the blank tape in the cassette holder. Check to make sure that all unloading and loading operations are correct.

Adjustment Diagram



TAPE TRANSPORT SYSTEM ADJUSTMENT

The transport system is the system in which tape moves from the supply reel disk, over the video head and then to the take-up reel disk. The components in the tape transport system must be perfectly clean, particularly those that come in contact with the tape.
These components must have no scratches, no dust, no oil on them. The tape transport system is adjusted at the factory prior to shipping. When components need to be replaced, accurately adjusting the new components ensures that the tape transport system will operate stably.



Components Adjusted in Tape Transport System

1. Reel Disk Height Adjustment

Purpose: Determine correct tape height by setting cassette tape reel to the specified height.

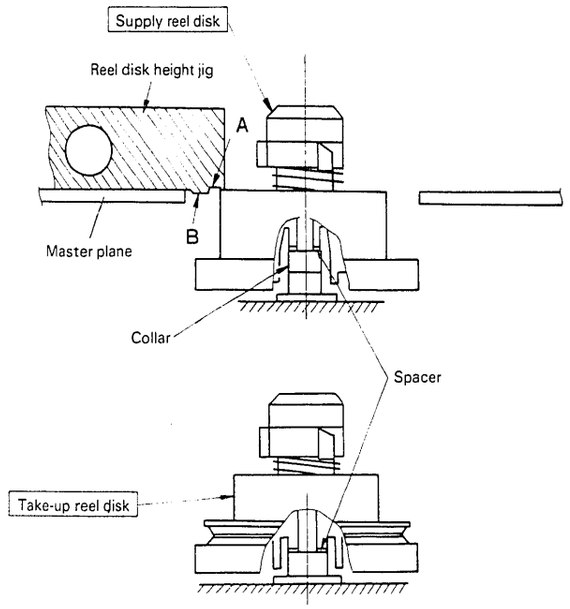
Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig	1) Remove chassis holder 2) Mount master plane and place reel disk height jig on it.	● Spacers in supply and take-up reel disks.

Adjustment Procedure

1) Make sure the reel disk is correctly positioned between points A and B on the reel disk height jig.
2) If the reel disk will not fit between points A and B, replace the spacer in the reel disk or adjust the number of spacers (0.25 mm and 0.5 mm thicknesses).

Caution:
If the tension arm/tension band have been removed, adjust the tension pole's position and tension after reassembling.

Adjustment Diagram



2. Tension/Tension Pole Position Adjustments

Purpose: Stabilize contact between video head and tape being supplied so that the tape tension is uniform throughout.

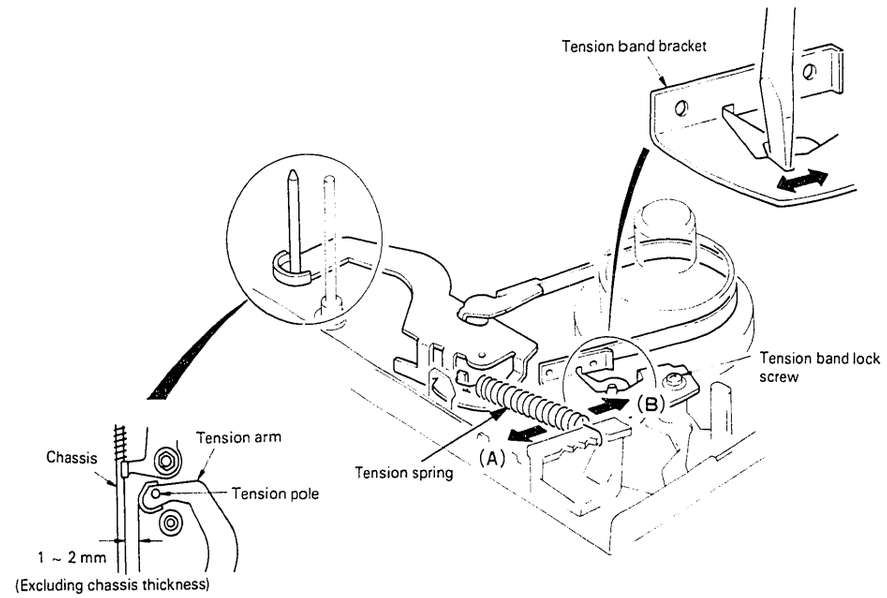
Test Equipment/Jigs	VTR State	Adjustment Point
● Flat-bladed screwdriver ● Tension cassette	1) Remove top cover 2) Place VTR in loading state without cassette insertion (see 4-17). **Tension adjustment** 3) Play tension cassette	**Position adjustment:** Tension band lock screw **Tension:** Tension spring hook position

Adjustment Procedure

Position Adjustment
1) Loosen lock screw on tension band. Insert flat bladed screwdriver in slot in bracket and chassis.
2) Use the screwdriver to slide the bracket for a 1 ~ 2 mm interval between the tension pole and chassis.
3) Tighten the lock screw on the tension band.
4) After adjusting, reload without inserting the tape and recheck the position of the tension pole.

Tension Adjustment
Reading of tension cassette:
30 ~ 40 g-cm. (reference value)
If tension is higher than the reference value, move the spring in direction A.
If tension is lower than the reference value, move the spring in direction B.
Caution: If a 6 g-cm or larger change is made in tension position, recheck tension pole position. If the position is off, readjust the tension pole's position and tension.

Adjustment Diagram



3. Guide Pole Height Adjustment

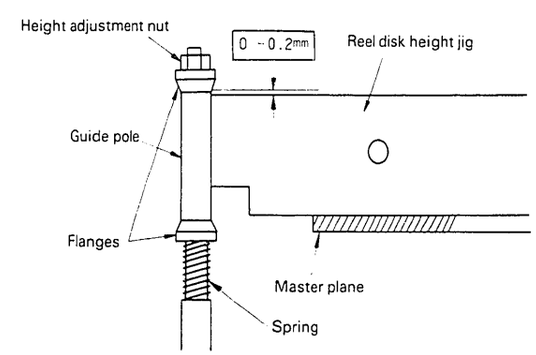
Purpose: Control tape height.

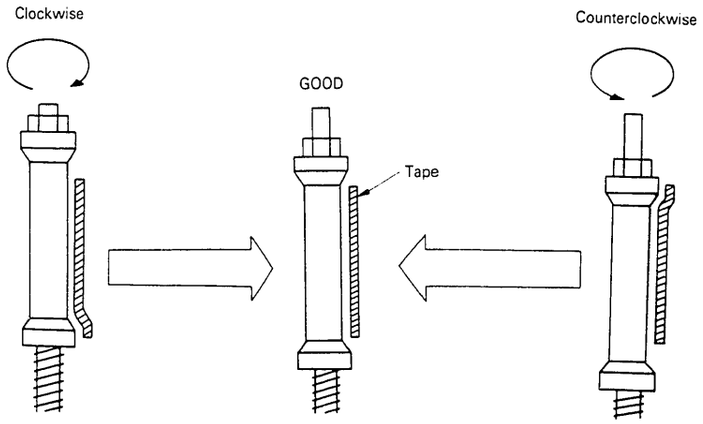
Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig ● Blank tape	1) Remove chassis holder 2) Mount master plane and place the reel disk height jig on it.	● Nut for adjusting height of supply and take-up guide poles (take-up pole is under cap).

Adjustment Procedure

1) Adjust gap between guide pole's upper flange and reel disk height jig to 0 ~ 0.2 mm.
2) Load and run the blank tape. Check to make sure the tape does not ride over the pole's upper or lower flange.
3) If the tape does ride over, adjust guide pole height.
   If tape rides over upper flange, turn adjustment nut counterclockwise.
   If tape rides over lower flange, turn adjustment nut clockwise.

Adjustment Diagram





4. Guide Roller Height Adjustments

Purpose: Control tape height so the tape's bottom edge runs along the cylinder's tape guideline.

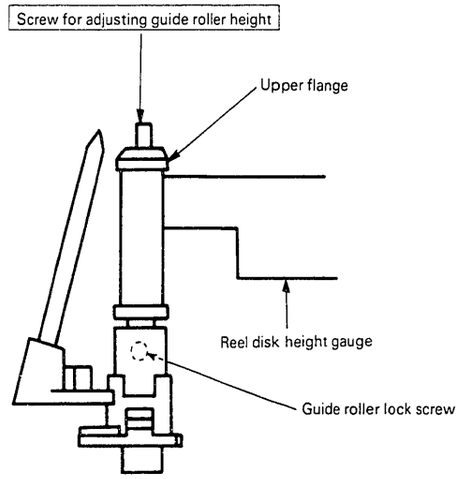
Coarse Adjustment

Test Equipment/Jigs	VTR State	Adjustment Point
● Master plane ● Reel disk height jig ● 1.5 mm hexagonal wrench	1) Remove chassis holder 2) Mount master plane and place reel disk height jig on it.	● Screws for adjusting height of supply and take-up guide rollers

Adjustment Procedure

1) Loosen guide roller lock screw so that the guide roller does not turn during loading, unloading and playback.
2) Set the upper edge of the reel disk height jig to the same level as the guide roller's upper flange.
3) Now make precision adjustments.

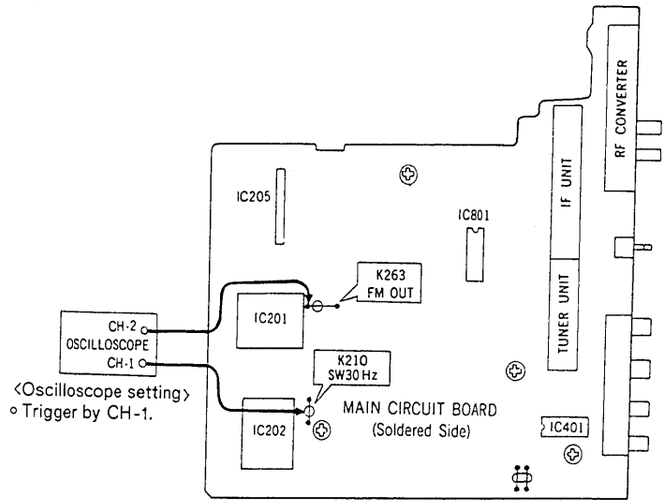
Adjustment Diagram



Precision Adjustment

Test Equipment/Jigs	Test Equipment Connection Points	VTR State	Adjustment Point
● Oscilloscope ● NTSC alignment tape ● Hexagonal wrench	● CH-1: K210 ● CH-2: K263	● Playback alignment tape	● Screw for adjusting guide roller height

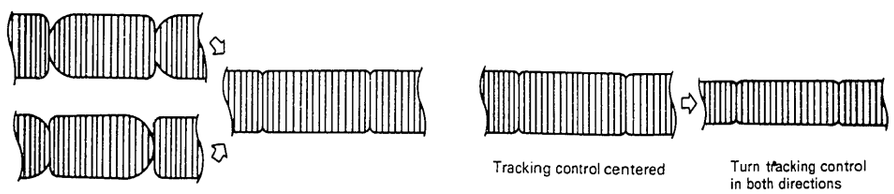
Connection Diagram



Adjustment Procedure

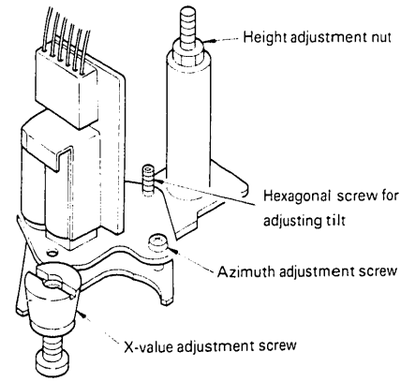
1) Tracking control: centered (when making this adjustment after replacing the cylinder, set the tracking control so the FM output is maximum.
2) Turn height adjustment screw to flatten the FM waveform.
3) Turn the tracking control both up and down.
4) Make sure that FM drops at the head and tail.
5) Tighten lock screw.

Waveform


Turn guide roller height adjustment screw
a little at a time to flatten waveform.
Tracking control centered
Turn tracking control
in both directions

5. Audio Control Head Adjustments

Purpose: Ensure uniform contact between tape and head to record and play a prescribed track.



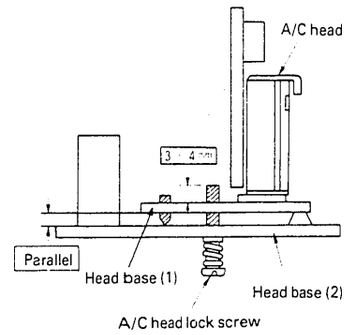
Coarse Adjustment

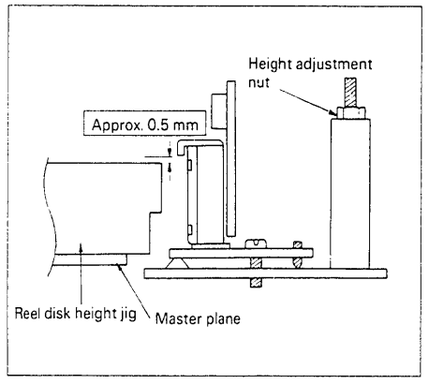
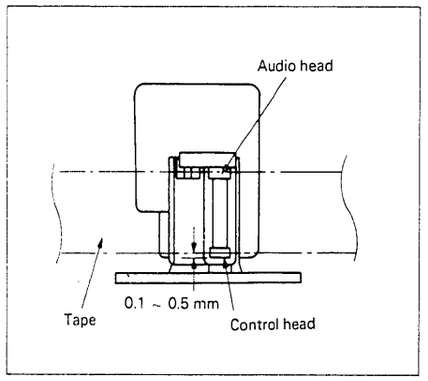
Test Equipment/Jigs	VTR State	Adjustment Points
● Master plane ● Reel disk height jig ● Blank tape ● Hexagonal wrench	1) Remove chassis holder 2) Mount master plane and place reel disk height jig on it.	● Azimuith adjustment screw ● Height adjustment nut ● Tilt adjustment screw

Adjustment Procedure

1) Tighten the A/C head lock screw through the spring from the bottom of head base (2) until the screw tip protrudes 3 ~ 4 mm from the top surface of head base (1).
2) Turn the tilt adjustment hexagonal screw and the azimuth adjustment screw so that head base (1) and head base (2) are parallel.

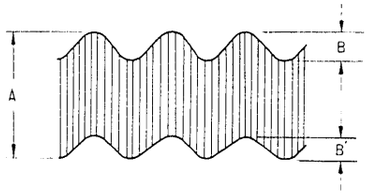
Adjustment Diagram



Adjustment Procedure	Adjustment Diagram
3) Turn the height adjustment nut until the gap between reel disk height jig and A/C head is approx. 0.5 mm.	
4) Remove the adjustment jigs and insert a blank tape. Place in playback mode. Make sure the tape does not curl or ride over around the A/C head. If the tape curls or rides over, readjust the tilt adjustment hex screw, the azimuth adjustment screw and the height adjustment nut. The ideal A/C head height is with the tap's bottom edge 0.1 ~ 0.15 mm from the bottom edge of the control head's core.	
5) Now move on to precision adjustments.	

Precision Adjustment

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Points
● Hexagonal wrench ● Oscilloscope ● NTSC Alignment tape	● Audio output jack	● Playback alignment tape (7 kHz portion)	● Azimuth adjustment screw ● Height adjustment nut ● Tilt adjustment screw

Adjustment Procedure	Waveform Diagram
1) Alternate turning, a little at a time, of the azimuth adjustment screw, the height adjustment nut and the tilt adjustment hex screw to both maximize and flatten audio output (minimize fluctuation).	 A: maximum BB': minimum

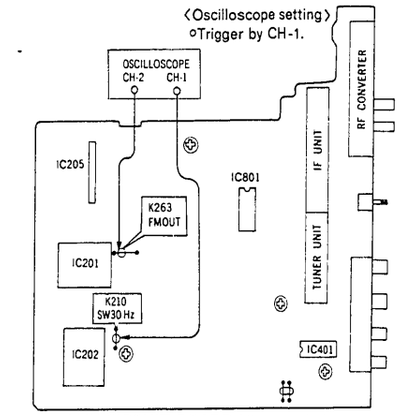
6. X Value Adjustment

Purpose: Ensure compatibility with other VTRs.

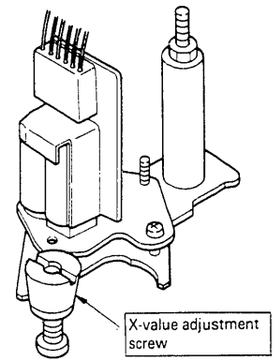
Caution: Be sure to adjust the tracking preset before making this adjustment.

Test Equipment/Jigs	Test Equipment Connection Point	VTR State	Adjustment Point
● Oscilloscope ● Alignment tape ● X-value adjustment screwdriver	● CH-1 : K210 ● CH-2 : K263	● Play back alignment tape (step wave portion)	● X-value adjustment screw

Connection Diagram



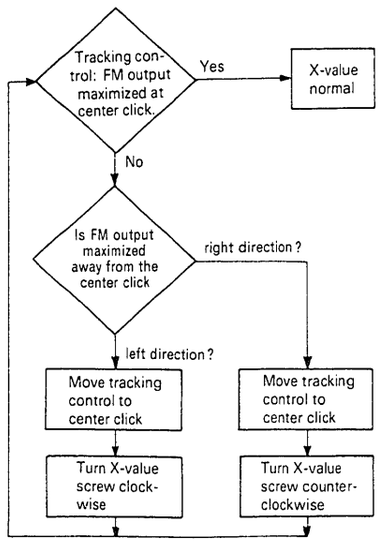
MAIN CIRCUIT BOARD (Soldered side)

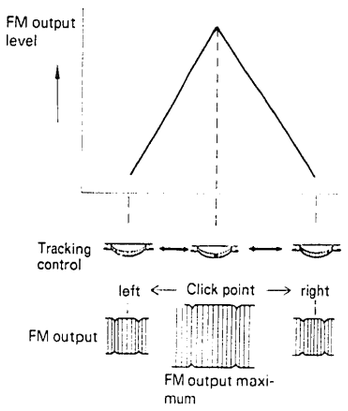


Adjustment Procedure

Adjustment using 30 HMP-2 alignment tape

Since the 30 μm head will trace over a 30 μm width track, center tracking control and make adjustments to maximize FM output.

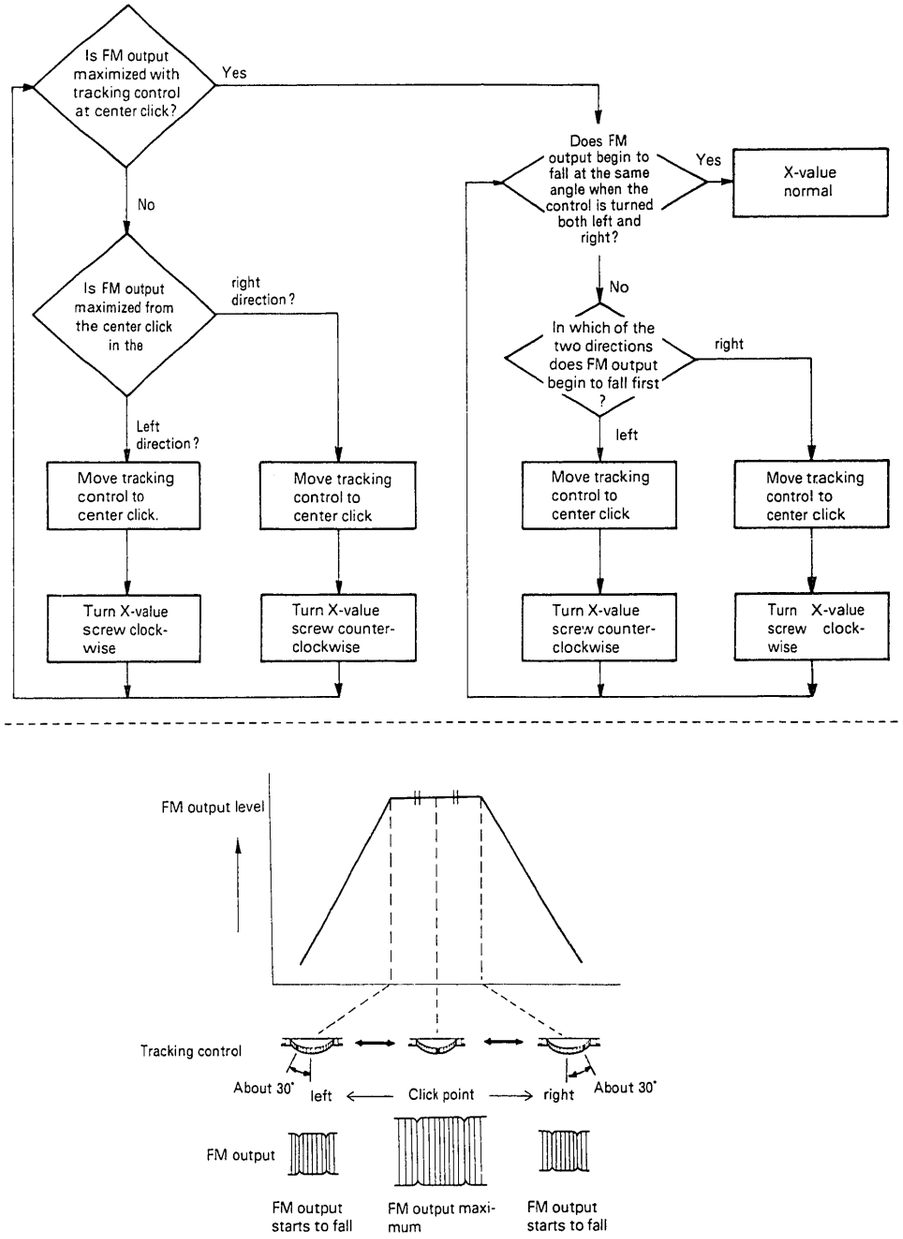

Tracking control: FM output maximized at center click.
Yes
X-value normal
No
Is FM output maximized away from the center click
right direction?
left direction?
Move tracking control to center click
Move tracking control to center click
Turn X-value screw clockwise
Turn X-value screw counterclockwise



Adjustment Procedure

Adjustment using NTSC alignment tape

Since the 60μm head will trace over a 60μm width track, center tracking control and make adjustments to maximize FM output, or turn the control both left and right about 30° and adjust so that FM output begins to fall at equivalent angles.

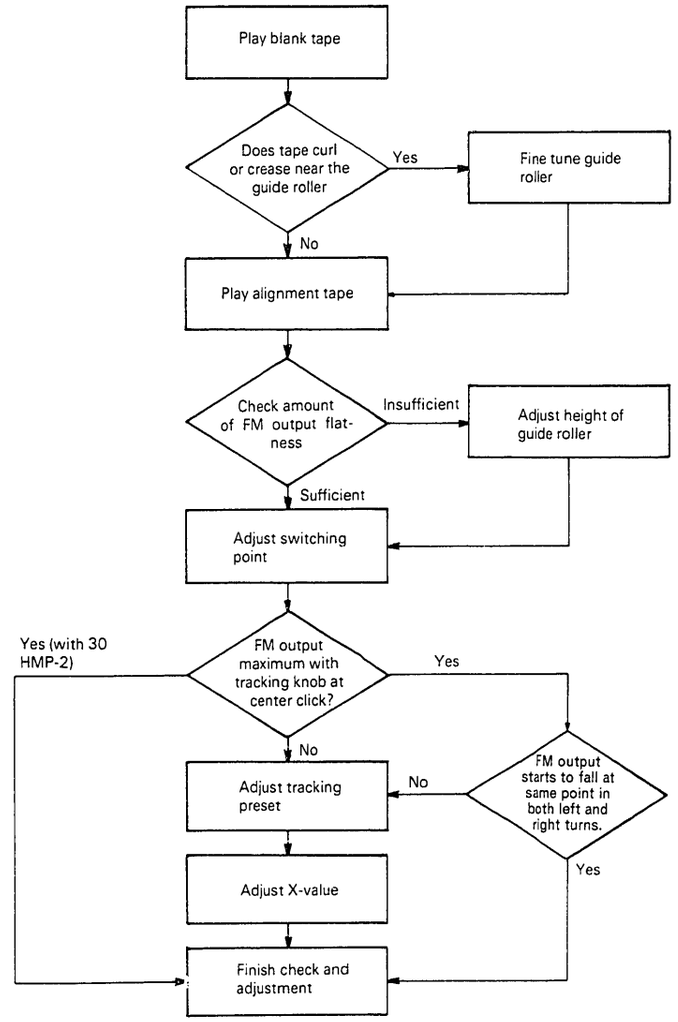

Is FM output maximized with tracking control at center click?
Yes
No
Is FM output maximized from the center click in the
right direction?
Left direction?
Move tracking control to center click.
Move tracking control to center click
Turn X-value screw clock-wise
Turn X-value screw counter-clockwise
Does FM output begin to fall at the same angle when the control is turned both left and right?
Yes
X-value normal
No
In which of the two directions does FM output begin to fall first ?
right
left
Move tracking control to center click
Move tracking control to center click
Turn X-value screw counter-clockwise
Turn X-value screw clock-wise
FM output level
Tracking control
About 30°
left
Click point
right
About 30°
FM output
FM output starts to fall
FM output maxi-mum
FM output starts to fall

7. Adjustments after replacing Cylinder (Video Head)

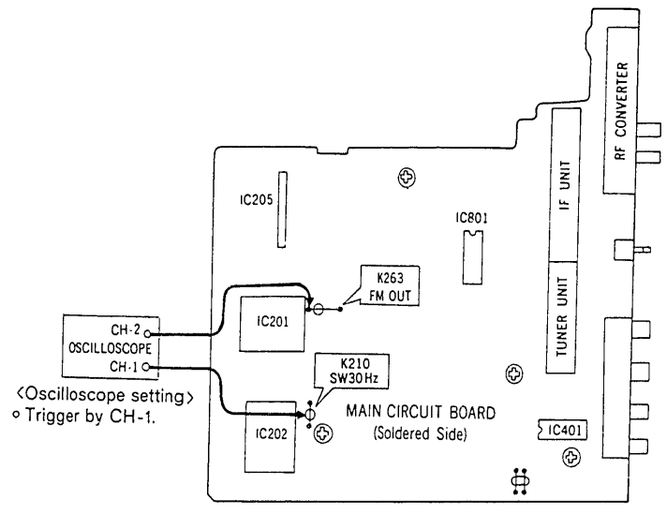
Purpose: A new replacement cylinder will differ with the guide roller in X-value and relative height. But, correct replacement procedures will reduce this disparity to a minimum.

Test Equipment/Jigs	Test Equipment Connection Points	Adjustment Points
● Oscilloscope ● Alignment tape ● Blank tape ● Hexagonal wrench ● X-value adjustment screwdriver	● Check amount of flattening ● CH-1 : K210 ● CH-2 : K263	● Guide roller (see precision adjustment on page 4-9) ● Switching point (see section 3) ● Tracking preset (see section 3) ● X-value (see page 4-12)

Check and Adjustment Procedures



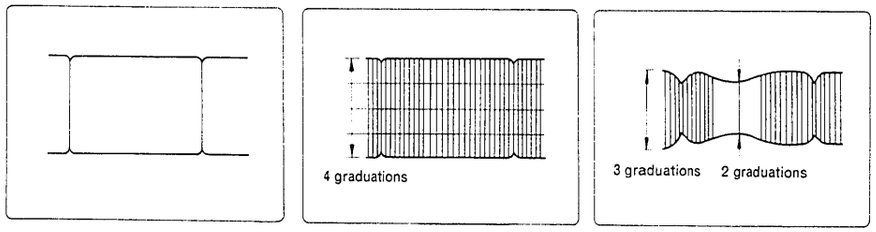
Connection Diagram



Procedures for checking amount of fluctuations and flatness in FM output

1) Use tracking control to maximize FM output.
2) Fine tune the oscilloscope's voltage level range to adjust FM output to 4 graduations.
3) Turn the tracking control to set the FM output's maximum amplitude at 3 graduations.
4) Make sure the minimum amplitude at this time is at 2 graduations or higher.
5) Make sure the difference between maximum and minimum level fluctuation is 13% or less.

Waveform Diagram



8. Checking Tension and Torque

Purpose: Checking tension, torque and pressure on the components that wind and move the tape is necessary to ensure smooth tape run and fulfill the VTR's basic functions. Make this check when tape run is rough or tape speed is incorrect.

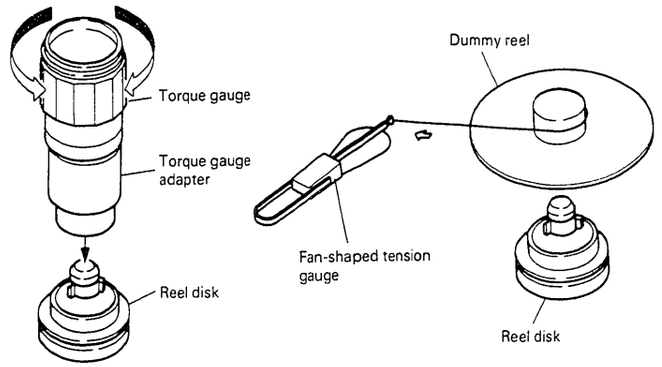
Test equipment/jigs	VTR state
● Torque gauge ● Torque gauge adapter ● Fan-shaped tension gauge ● Dummy reel	● Operate VTR without loading tape cassette (see page 4-17)

Item	VTR Operation mode	Measurement reel	Measurement values	Remarks
Main brake torque	Stop	Supply and take-up reels	170 g·cm or more	Note 1
Slack removal torque	Unloading	Supply reel	90 ~ 190 g·cm	Note 1
Fast forward torque	Fast forward	Take-up reel	400 g·cm or more	Note 1
Rewind torque	Rewind	Supply reel	400 g·cm or more	Note 1
Reel winding torque	Play	Take-up reel	90 ~ 180 g·cm	Note 1
Back-tension torque	Fast forward	Supply reel	4 ~ 15 g·cm	Note 2
	Rewind	Take-up reel		

Note: 1. Value when using torque gauge and torque gauge adapter for measurement with torque gauge sliding at 0.8 rps. However, main brake torque indicates measurement values during manual rotation of take-up reel, counterclockwise, and supply reel, clockwise, at 0.8 rps.

Note: 2. Indicates the value when the dummy reel and fan-shaped tension gauge are used to measure the take-up reel disk pulling counterclockwise and the supply reel disk pulling clockwise at 50 mm/s.

Adjustment Diagram

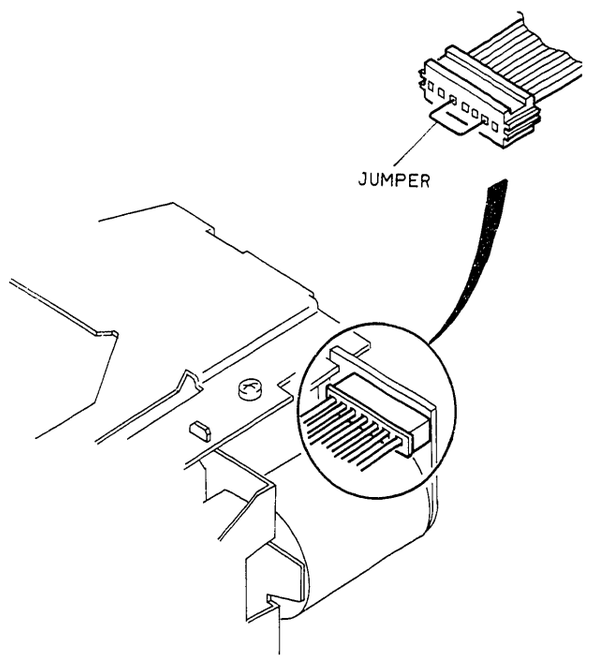


Note: Method with VTR in loading state and no tape cassette inserted.

1) Remove top cover.
2) Remove AC plug from wall socket.
3) Disconnect the connector from the plug (PG-4) on the cassette loading motor circuit board.
4) Short-circuit pins 2 and 5 of the connector.
5) Insert AC plug into wall socket.
6) Turn VTR power on.
   In this state, the VTR will accept all modes. However, rewind can be performed for only a few seconds because the take-up disk is in stop state and reel pulses cannot be detected.

[Caution]
After the aboved operations, always use the following steps to return to the original modes.

1) Remove short-circuit from connector and insert in plug.
2) Remove the AC plug from the wall socket once to reset the system control microprocessor.

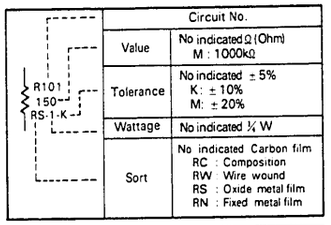


CHAPTER 5

SCHEMATIC/CIRCUIT BOARD DIAGRAM

Note

1. Voltage measured at base of chassis with minimum volume control and no signal.
   ( ) are shown in recording condition.
2. Nomenclature of Resistors and Capacitors.

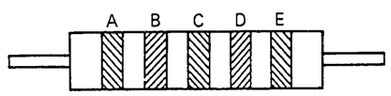


Circuit No.		
Value	No indicated Ω (Ohm) M : 1000kΩ	
Tolerance	No indicated ± 5% K: ± 10% M: ± 20%	
Wattage	No indicated ¼ W	
Sort	No indicated Carbon film RC : Composition RW : Wire wound RS : Oxide metal film RN : Fixed metal film	
Circuit No.		
Value	No indicated μF P : PF	
Tolerance	No indicated ± 10% J : ± 5% M: ± 20% Z : +80% – 20% D : ± 0.5pF C : ± 0.25pF	
Sort	⊣⊢	Ceramic
	+⊣⊢	Electrolitic
	M⊣⊢	Mylar
	P⊣⊢	Polyester
	S⊣⊢	Styrol
Voltage	No indicated 50WV	

3. Be sure to make your orders of resistors and capacitors with value, voltage, tolerance and sort.
4. When replacing capacitors marked With * use specified ones stated on parts list since required temperature characteristics.

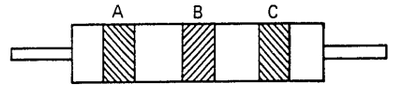
HOW TO READ CAPACITY AND INDUCTANCE OF RESISTOR SHAPE CAPACITORS AND COILS

CAPACITOR



CAPACITY: (10A+B)xC [PF]
TOLERANCE: D
RATED VOLTAGE: BODY COLOR
Pink: 25V
Green: 50V
CHARACTERISTICS: E

COIL



INDUCTANCE: (10A+B)xC [μH]

COLOR	A, B	C	D	E
Black	0	10^0	±20%	For temperature compensation
Brown	1	10^1		
Red	2	10^2		
Orange	3	10^3		
Yellow	4	10^4		
Green	5	10^5		
Blue	6			
Violet	7			
Grey	8		±30%	High dielectric constant type
White	9			For temperature compensation
Gold		10^{-1}	± 5%	
Silver		10^{-2}	±10%	High dielectric constant type

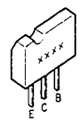
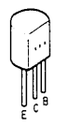
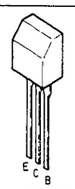
Cautions on use of MOS IC

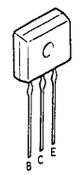
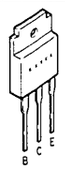
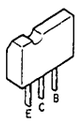
1. The MOS IC is inserted in black foam for shipment. This foam is a conductor which short-circuits between the leads to prevent damage. Do not remove ICs from this foam during their storage. Avoid removing ICs from this foam, placing them on plastic which is likely to be charged with static electricity or inserting them into styrol foam.
2. High voltages may be applied during doldering caused by leakages from the soldering iron, so be sure to ground the tip of the soldering iron or use a low voltage soldering iron.
3. The human body, clothes made of synthetic fibres or nylon gloves may be charged with several thousands volts of static electricity because of friction, so a workers should be grounded.
4. Be sure to ground measuring instruments such as oscilloscopes, VTVMs, etc. used for repairs.

SEMICONDUCTOR CONFIGURATION

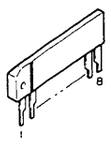
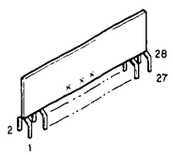
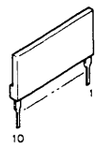
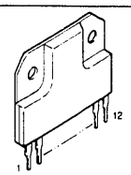
When replacing a semiconductor, take care of its pin numbers and markings (recess, paint) so as not to insert it in reverse.

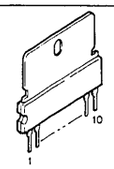
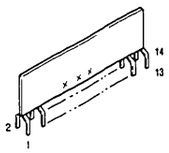
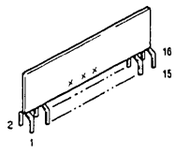
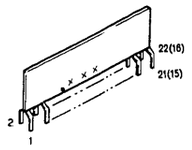
TRANSISTOR

1	2	3	4
			
2SC2021	2SA673 2SA952 2SB562 2SD468 2SC458	2SA844	2SC1740 DTA124 DTC124 DTA144 DTC144

5	6	7
		
2SC2784 2SC3553 2SD1504	2SD1266	2SA874

IC (SINGLE INLINE PACKAGE)

1	2	3	4
			
LA7016	HT4763	STK5471	M54648L

5	6	7	8
			
M54649L	M51485L	HA11888	HA13403(22P) HA11887(16P)

IC (DUAL INLINE PACKAGE)

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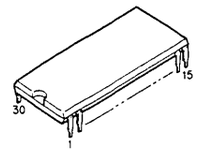
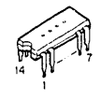
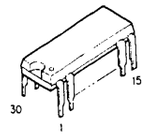
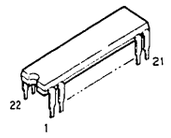
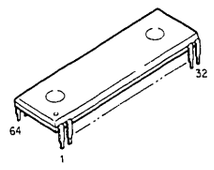
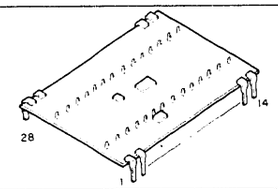
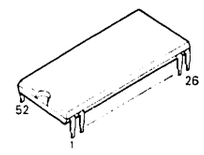
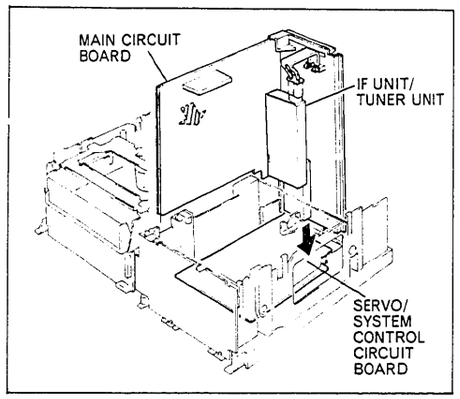
			
M50161	M58657	M51654P	LA7935

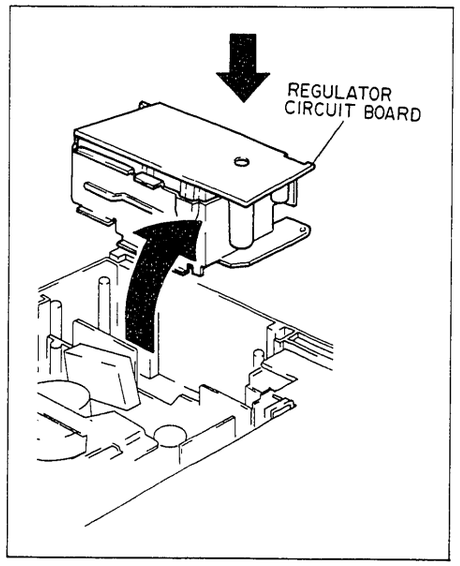
5	6	7
		
HA11853 HD614042S	HT4765 HT4706	M50752

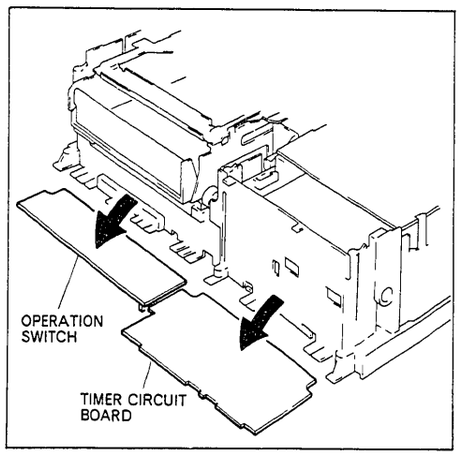
CIRCUIT BOARD CONFIGURATION

No.	CIRCUIT BOARD	PAGE	SCHEMATIC	PAGE
1	PREAMP	——	PREAMP	5-11
2	REGULATOR (VT-1105A) REGULATOR (VT-1100AR)	5-41 5-45	REGULATOR (VT-1105A) REGULATOR (VT-1100AR)	5-39 5-43
3	MAIN	5-19	V.S TUNING	5- 7
			AUDIO	5- 9
			LUMINANCE/CHROMA	5-12
4	TIMER	5-21	TIMER/OPERATION SWITCH	5-23
5	OPERATION SWITCH	5-21		
6	SERVO/SYSTEM CONTROL	5-37	SYSTEM CONTROL	5-29
			SERVO	5-32

HOW TO CHECK THE CIRCUIT BOARD

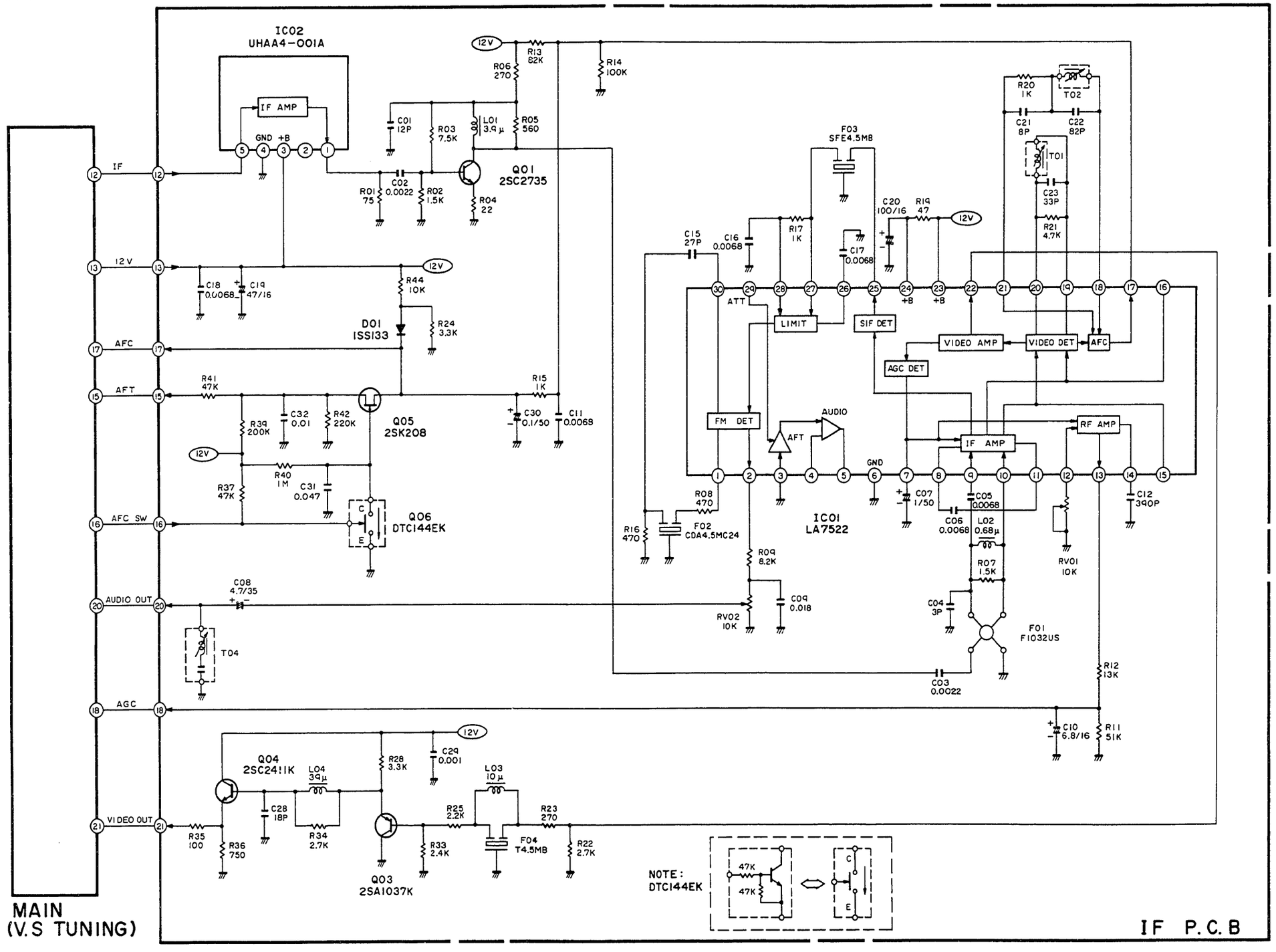






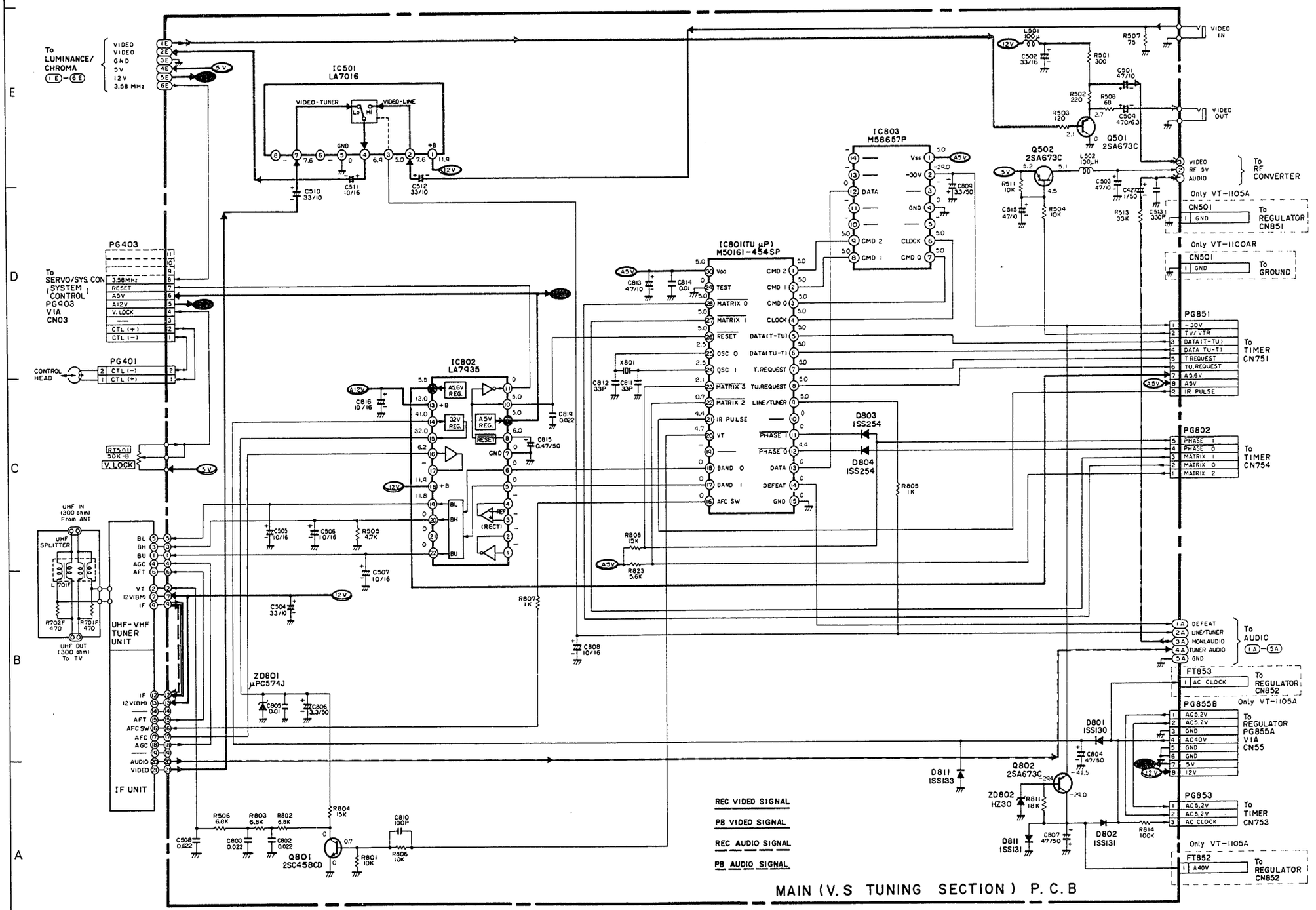
SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

IF UNIT



IF UNIT 5-5 5-6 IF UNIT

V.S TUNING



※ ONE VOLTAGE:PB OR REC MODE.

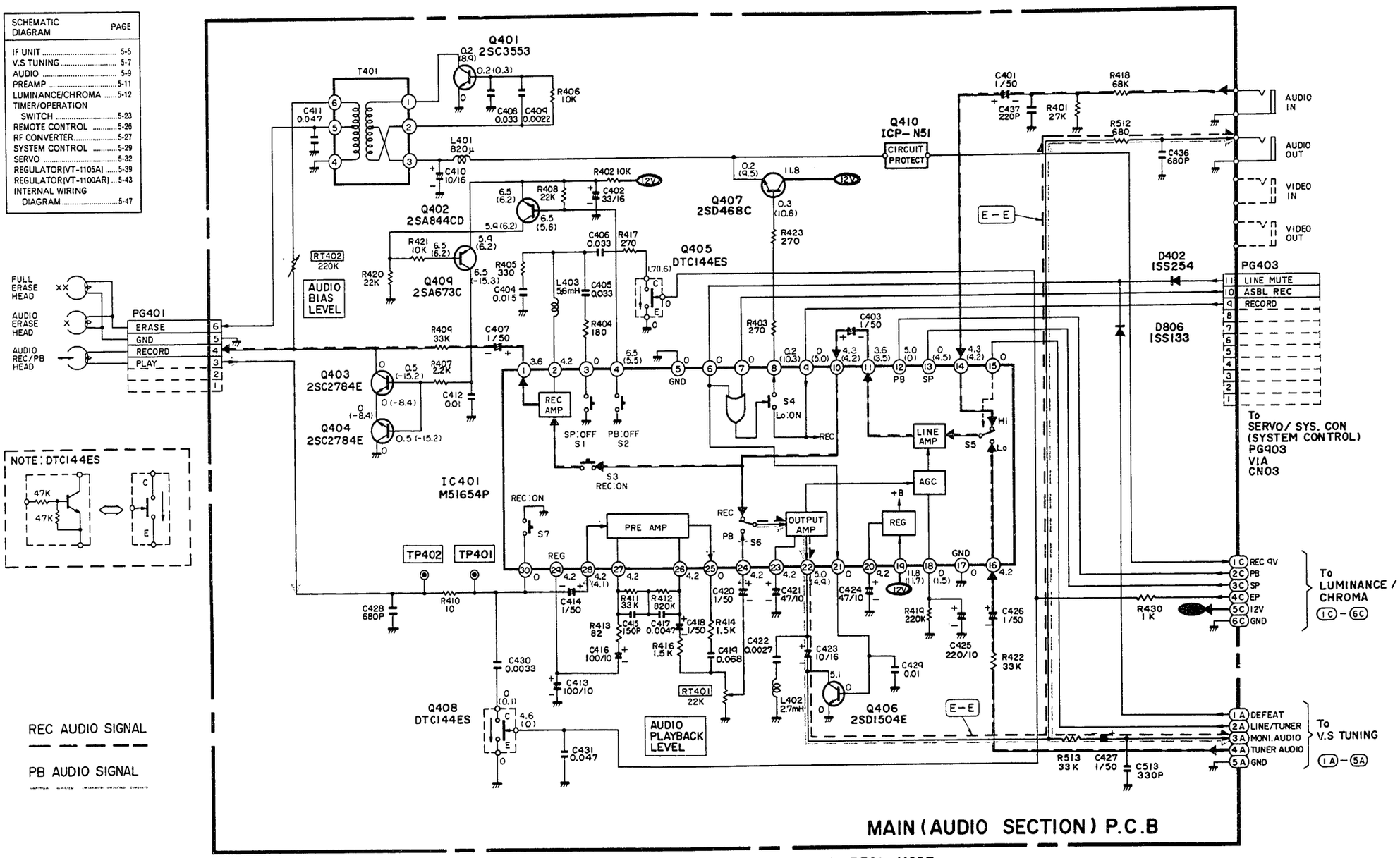
AUDIO

SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR(VT-1105A)	5-39
REGULATOR(VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

NOTE: DTC144ES

REC AUDIO SIGNAL

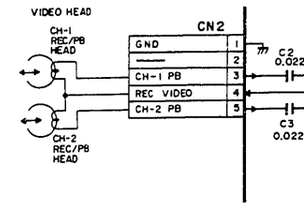
PB AUDIO SIGNAL

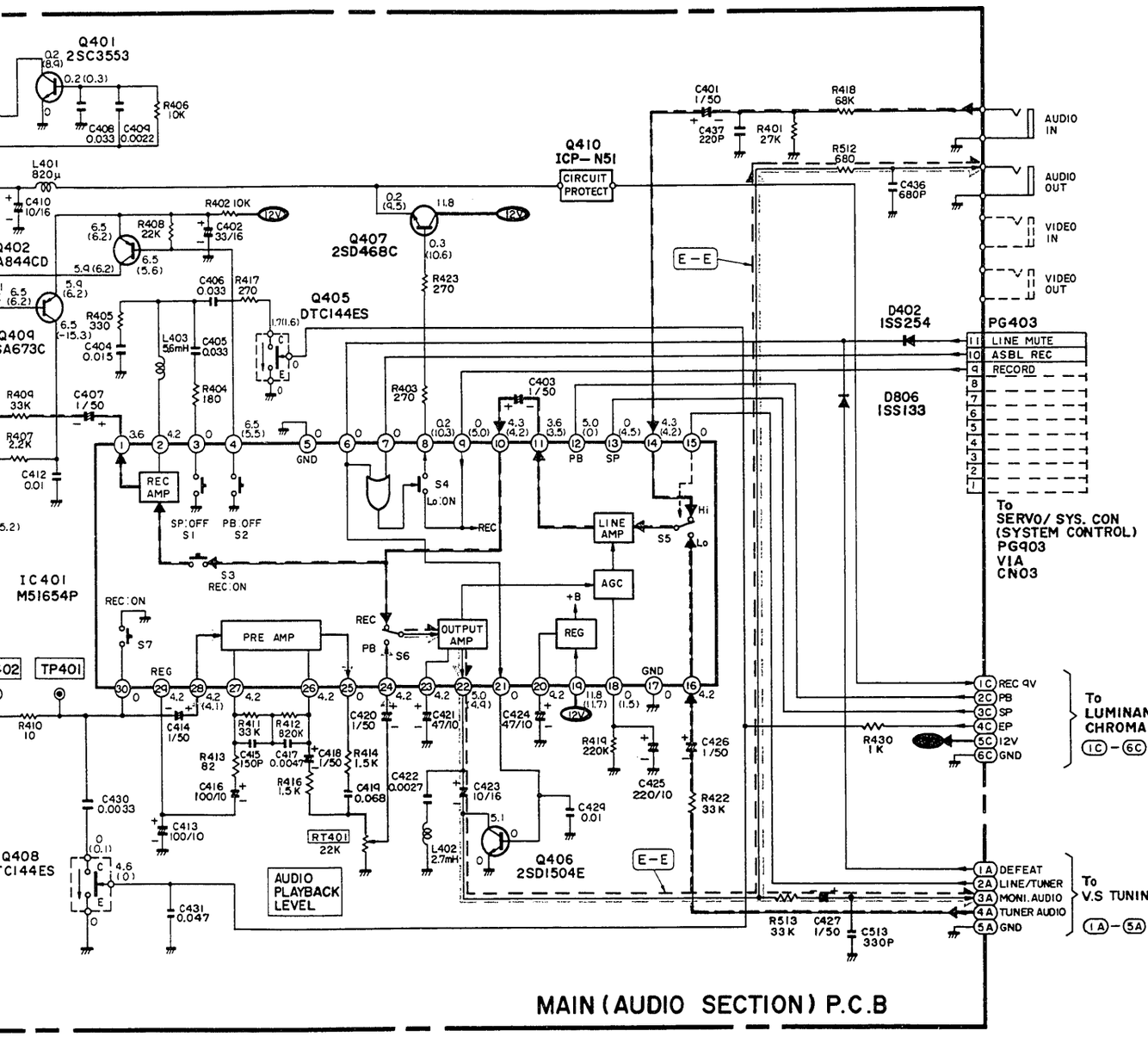


MAIN (AUDIO SECTION) P.C.B

※ ONE VOLTAGE : PB OR REC MODE, TWO VOLTAGES: PB AND (REC) MODE.

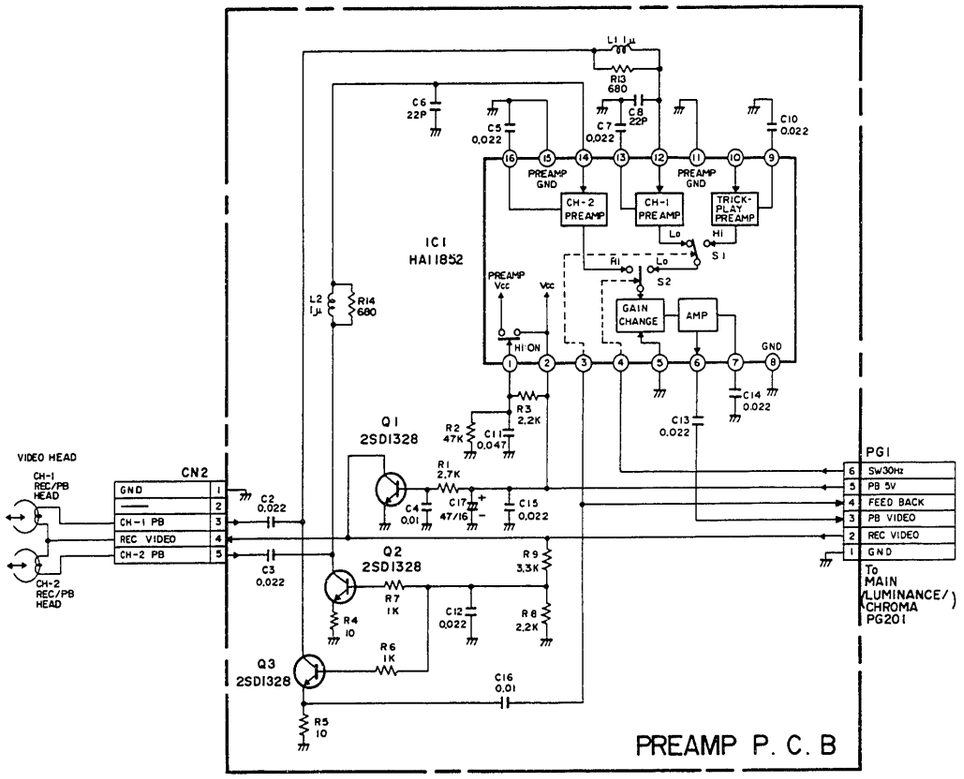
PREAMP





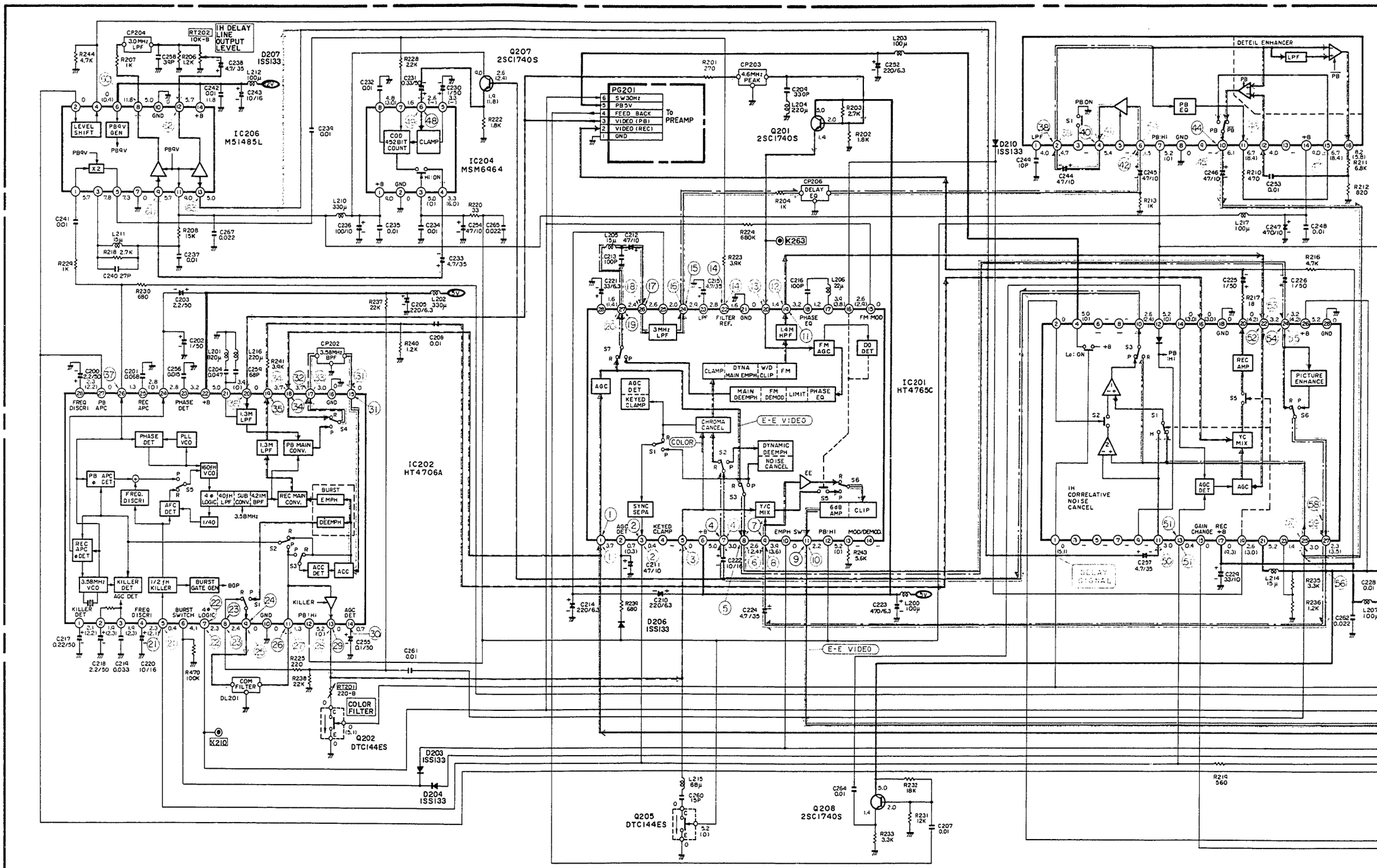
VOLTAGE : PB OR REC MODE, TWO VOLTAGES: PB AND (REC) MODE.

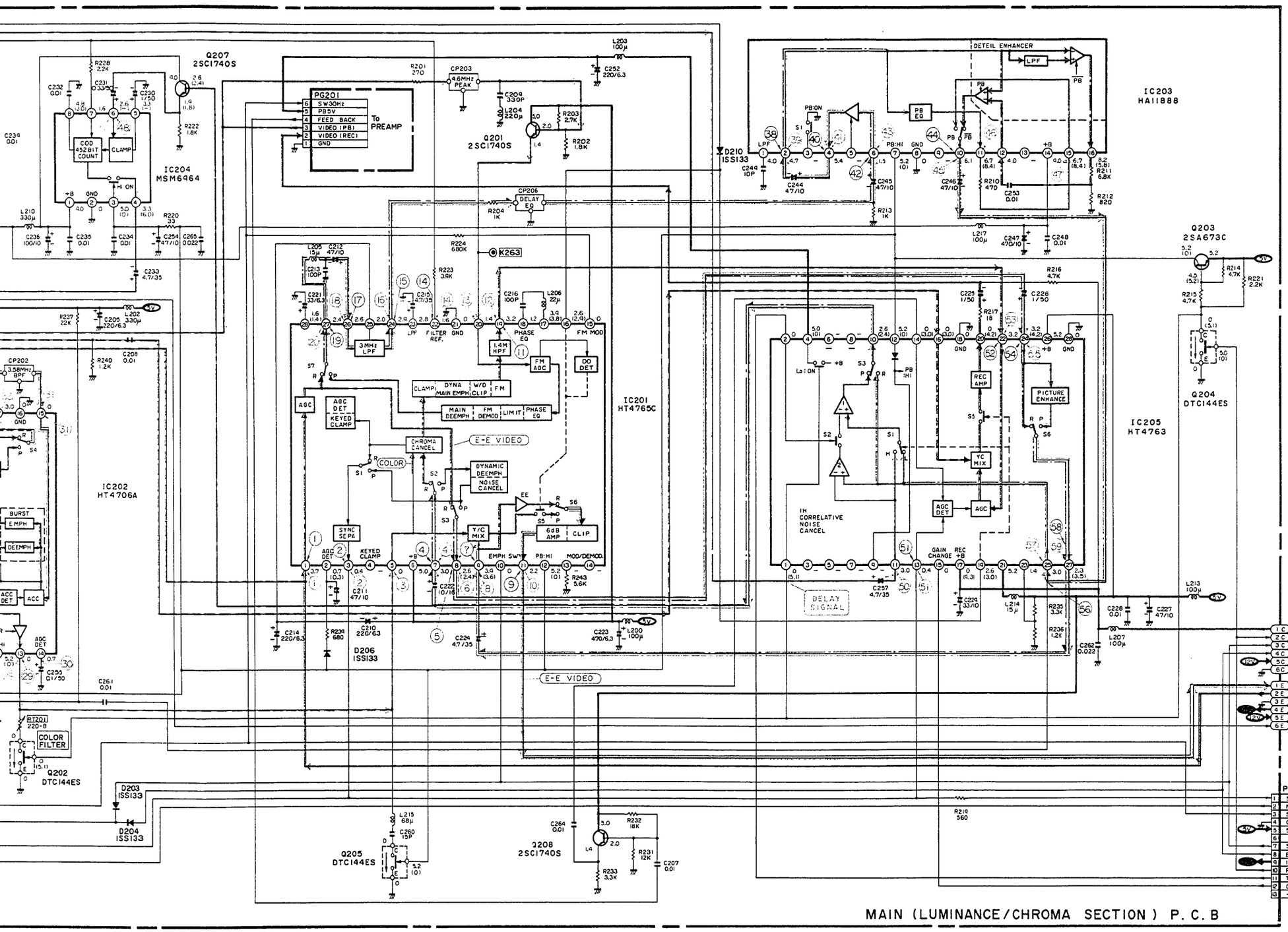
PREAMP



SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR(VT-1105A)	5-39
REGULATOR(VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

LUMINANCE/CHROMA





MAIN (LUMINANCE/CHROMA SECTION) P.C.B

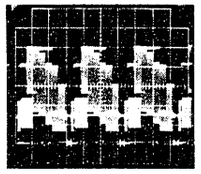
SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR(VT-1105A)	5-39
REGULATOR(VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

OR REC MODE, TWO VOLTAGES: PB AND (REC) MODE.

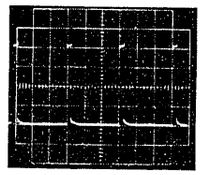
LUMINANCE/CHROMA CIRCUIT WAVEFO

[IC201] (REC : Color bar 1Vp-p Video IN/PB : NTSC Alignment tape)

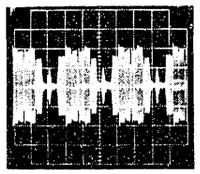
① PIN 1 REC/PLAY
0.2V/10μs div.



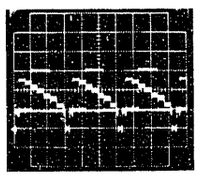
② PIN 3 REC/PLAY
1V/20μs. div.



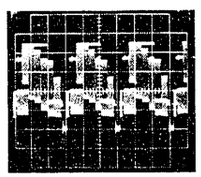
③ PIN 5 PLAY
50mV/20μs. div.



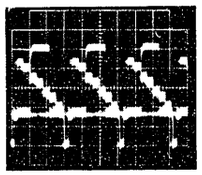
④ PIN 7 REC/PLAY
0.1V/20μs. div.



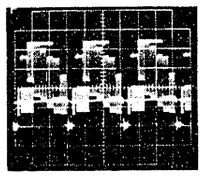
⑤ PIN 8 REC
50mV/20μs. div.



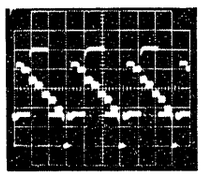
⑥ PIN 8 PLAY
0.2V/20μs. div.



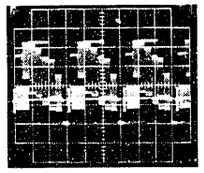
⑦ PIN 9 REC
50mV/20μs. div.



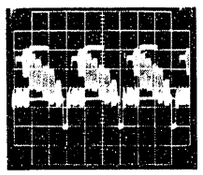
⑧ PIN 9 PLAY
0.2V/20μs. div.



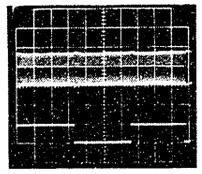
⑨ PIN 11 REC
0.5V/20μs. div.



⑩ PIN 11 PLAY
0.5V/20μs. div.

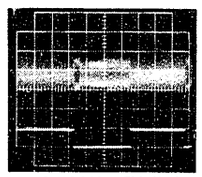


⑪ PIN 19 REC
0.2V/5ms. div.



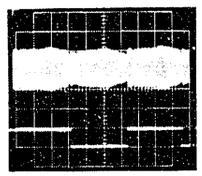
(SW30Hz : 5V div.)

⑫ PIN 19 PLAY
0.2V/5ms. div.



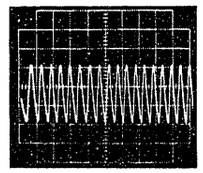
(SW30Hz : 5V div.)

⑬ PIN 20 PLAY
0.1V/5ms. div.

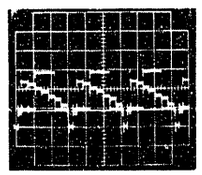


(SW30Hz : 5V div.)

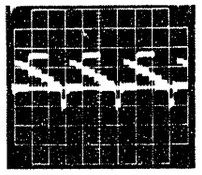
⑭ PIN 22 REC/PLAY
50mV/5ms. div.



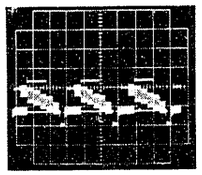
⑮ PIN 24 REC
0.2V/20μs. div.



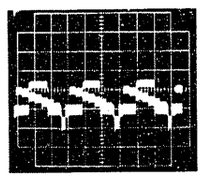
⑯ PIN 24 PLAY
0.2V/20μs. div.



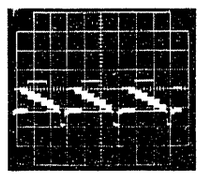
⑰ PIN 26 REC
0.1V/20μs. div.



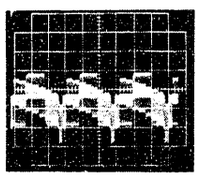
⑱ PIN 26 PLAY
0.1V/20μs. div.



⑲ PIN 27 REC
50mV/20μs. div.

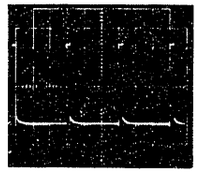


⑳ PIN 27 PLAY
0.1V/20μs. div.

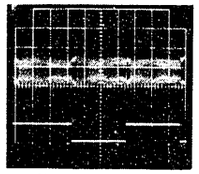


[IC202]

㉑ PIN 5 REC/PLAY
1V/20μs. div.

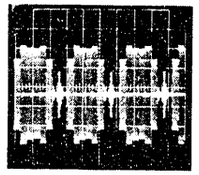


㉖ PIN 11 REC
10mV/5ms. div.



(SW 30Hz: 5V div.)

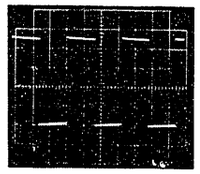
㉛ PIN 15 REC/PLAY
50mV/20μs. div.



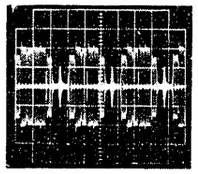
㊱ PIN 20 PLAY
0.2V/5ms. div.

(SW 30Hz: 5V div.)

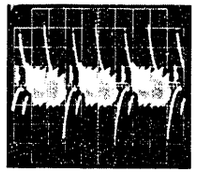
㉒ PIN 7 REC/PLAY
1V/5ms. div.



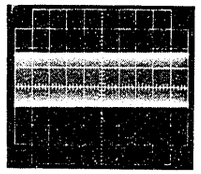
㉗ PIN 11 PLAY
50mV/20μs. div.



㉜ PIN 17 REC
0.2V/20μs. div.



㊲ PIN 26 REC
0.1V/20μs. div.



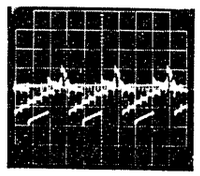
㉓ PIN 8 REC/PLAY
0.1V/20μs. div.

㉘ PIN 13 PLAY
50mV/20μs. div.

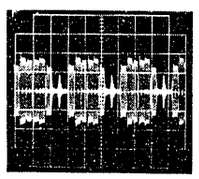
㉝ PIN 17 PLAY
0.2V/20μs. div.

(SW 30Hz: 5V div.)

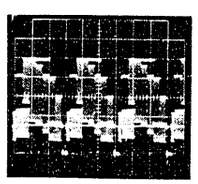
㉔ PIN 9 REC
0.1V/20μs. div.



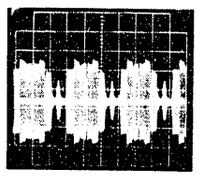
㉙ PIN 13 REC
20mV/5μs. div.



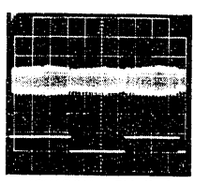
㉞ PIN 18 REC/PLAY
0.2V/20μs. div.



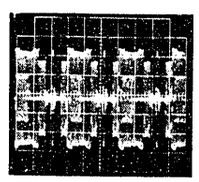
㉕ PIN 9 PLAY
0.1V/20μs. div.



㉚ PIN 14 REC
20mV/5μs. div.



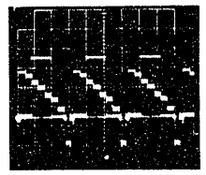
㉟ PIN 19 REC
0.1V/20μs. div.



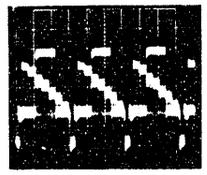
(SW 30Hz: 5V div.)

[IC203]

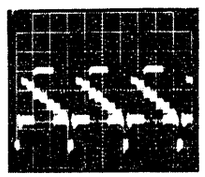
㊳ PIN 2 REC
0.2V/20μs. div.



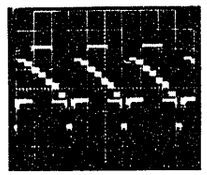
㊸ PIN 6 PLAY
50mV/20μs. div.



㊴ PIN 2 PLAY
0.2V/20μs. div.



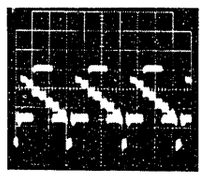
㊹ PIN 10 REC
0.1V/20μs. div.



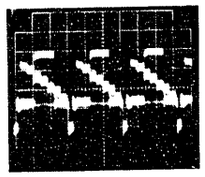
㊵ PIN 4 REC
0.2V/20μs. div.

㊺ PIN 10 PLAY
0.1V/20μs. div.

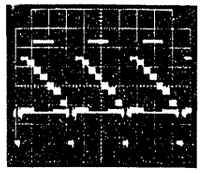
㊶ PIN 4 PLAY
0.2V/20μs. div.



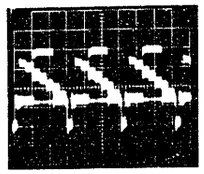
㊻ PIN 11 PLAY
0.1V/20μs. div.



㊷ PIN 6 REC
50mV/20μs. div.

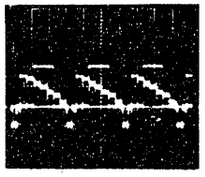


㊼ PIN 15 PLAY
0.1V/20μs. div.

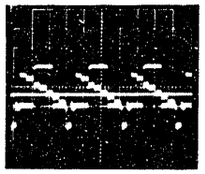


[IC204]

㊽ PIN 6 REC
0.1V/20μs. div.

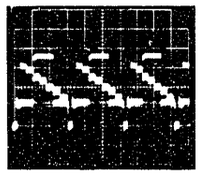


㊾ PIN 6 PLAY
0.1V/20μs. div.

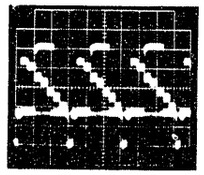


[IC205]

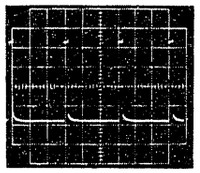
⑤⓪ PIN 11 PLAY
0.1V/20μs. div.



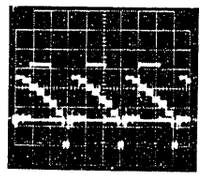
⑤⑤ PIN 24 PLAY
0.2V/20μs. div.



⑤① PIN 13 REC/PLAY
1V/20μs. div.



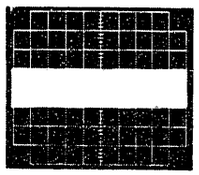
⑤⑥ PIN 25 REC
0.1V/20μs. div.



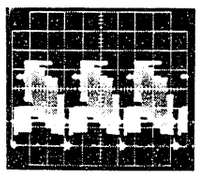
⑤② PIN 22 REC
0.2V/20μs. div.

⑤⑦ PIN 25 PLAY
0.1V/20μs. div.

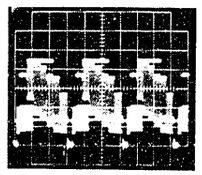
⑤③ PIN 22 PLAY
0.2V/20μs. div.



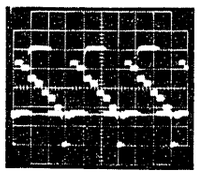
⑤⑧ PIN 27 REC
50mV/20μs. div.



⑤④ PIN 24 REC
50mV/20μs. div.

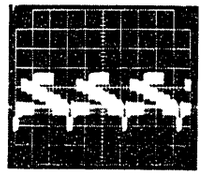


⑤⑨ PIN 27 PLAY
0.2V/20μs. div.

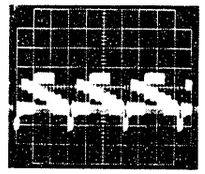


[IC206]

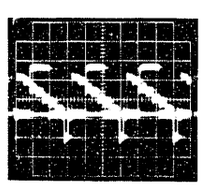
⑥⓪ PIN 8 PLAY
0.5V/20μs. div.



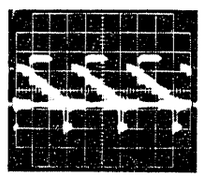
⑥① PIN 9 PLAY
0.5V/20μs. div.



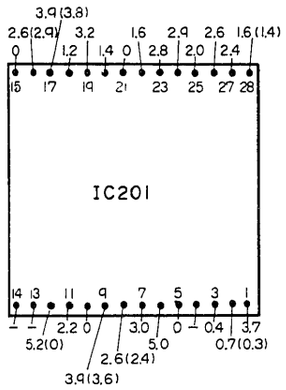
⑥② PIN 12 PLAY
0.1V/20μs. div.

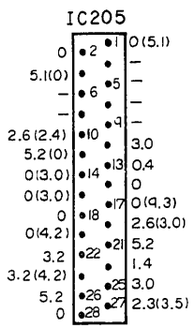


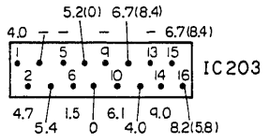
⑥③ PIN 13 PLAY
0.1V/20μs. div.

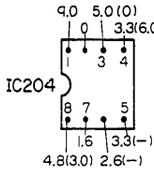


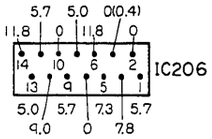
MAIN

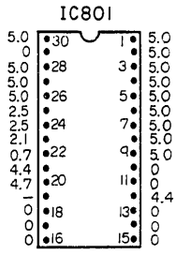












RT202
1H DELAY LINE OUTPUT LEVEL

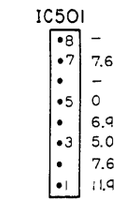
VT-1100AR Only
CN501 To GROUND

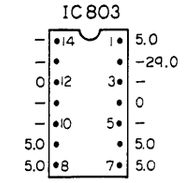
VT-1105A Only
CN501 To REGULATOR CN851

RF CONVERTER
① AUDIO
② RF 5V
③ VIDEO

IF UNIT
(21) VIDEO
(20) AUDIO
(19) —
(18) AGC
(17) AFC
(16) AFC SW
(15) AFT
(13) 12V (BM)
(12) IF

TUNER UNIT
(9) IF
(7) 12V(BM)
(6) AFT
(5) BL
(4) AGC
(3) BH





V. LOCK

To TIMER CN751

To TIMER CN702

To SERVO/SYS. CON (SERVO) PG604

To SERVO/SYS. CON. (SYSTEM CONTROL) PG903

To FULL ERASE HEAD/ AUDIO ERASE HEAD/ AUDIO REC/PB HEAD

PG201 To PRE AMP

PG802

PG851

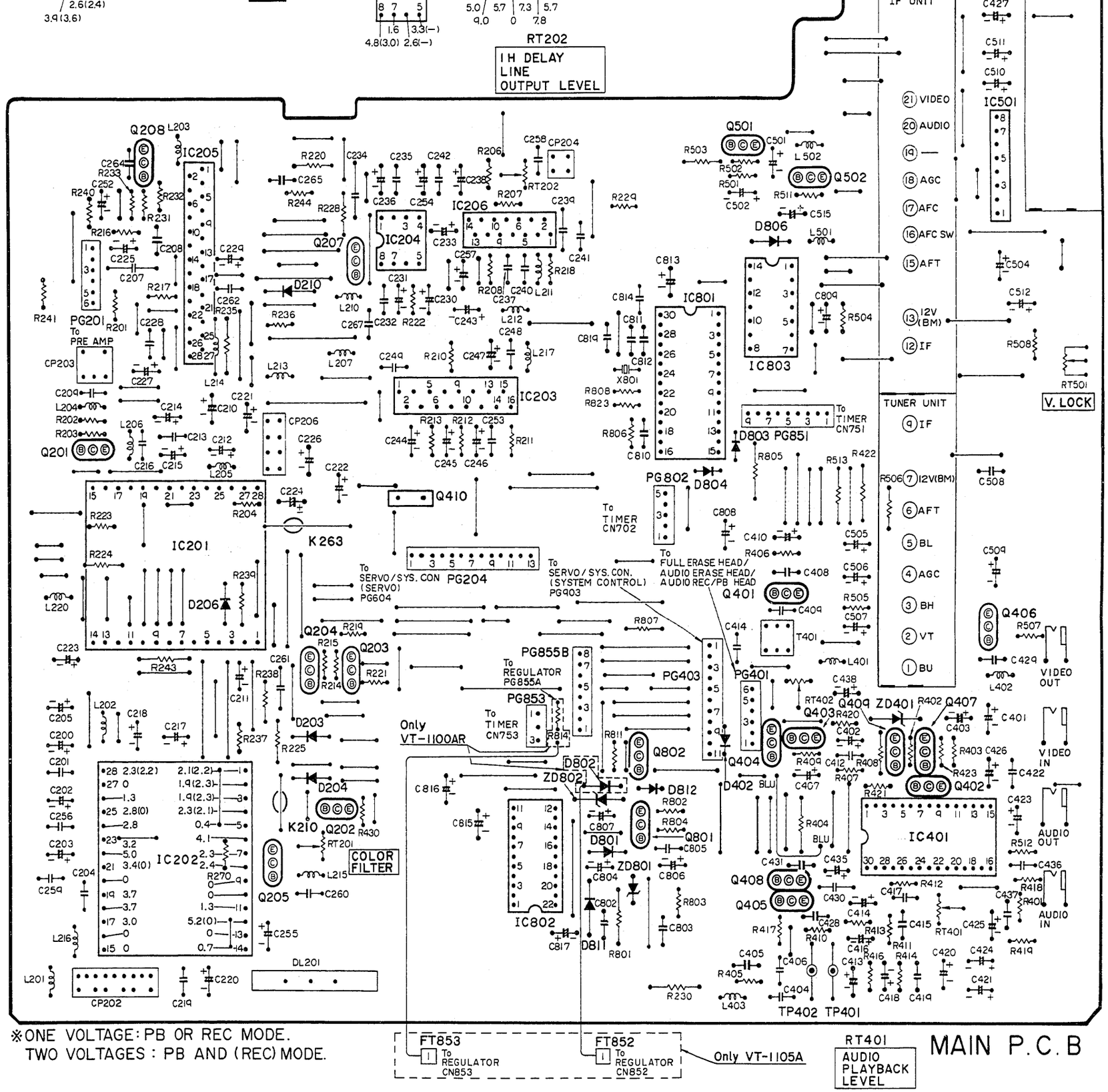
K263

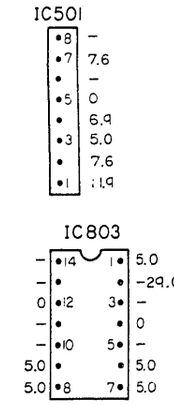
Q208 Q207 Q201 Q410 Q501 Q502 Q401 Q406

D210 D206 D806 D804 D803

X801

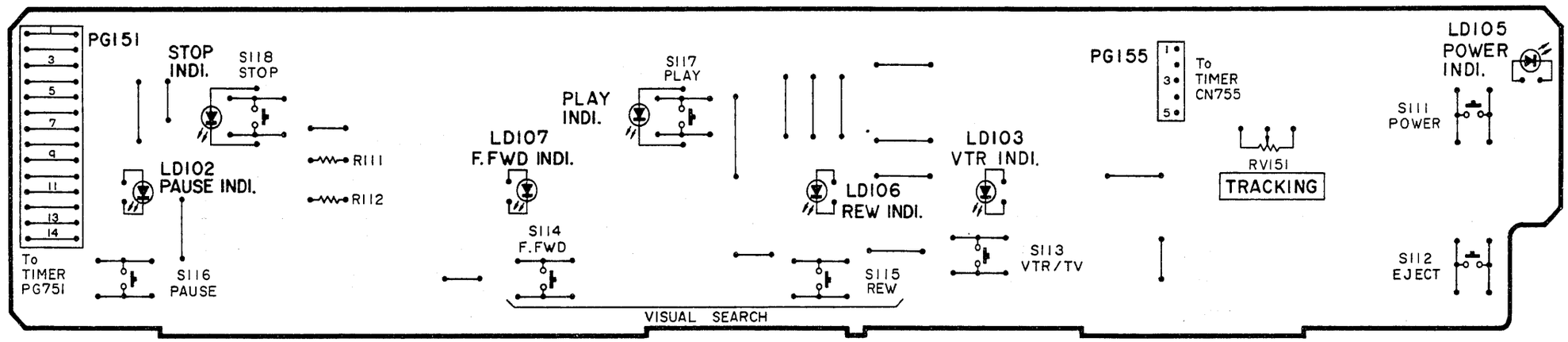
RT501





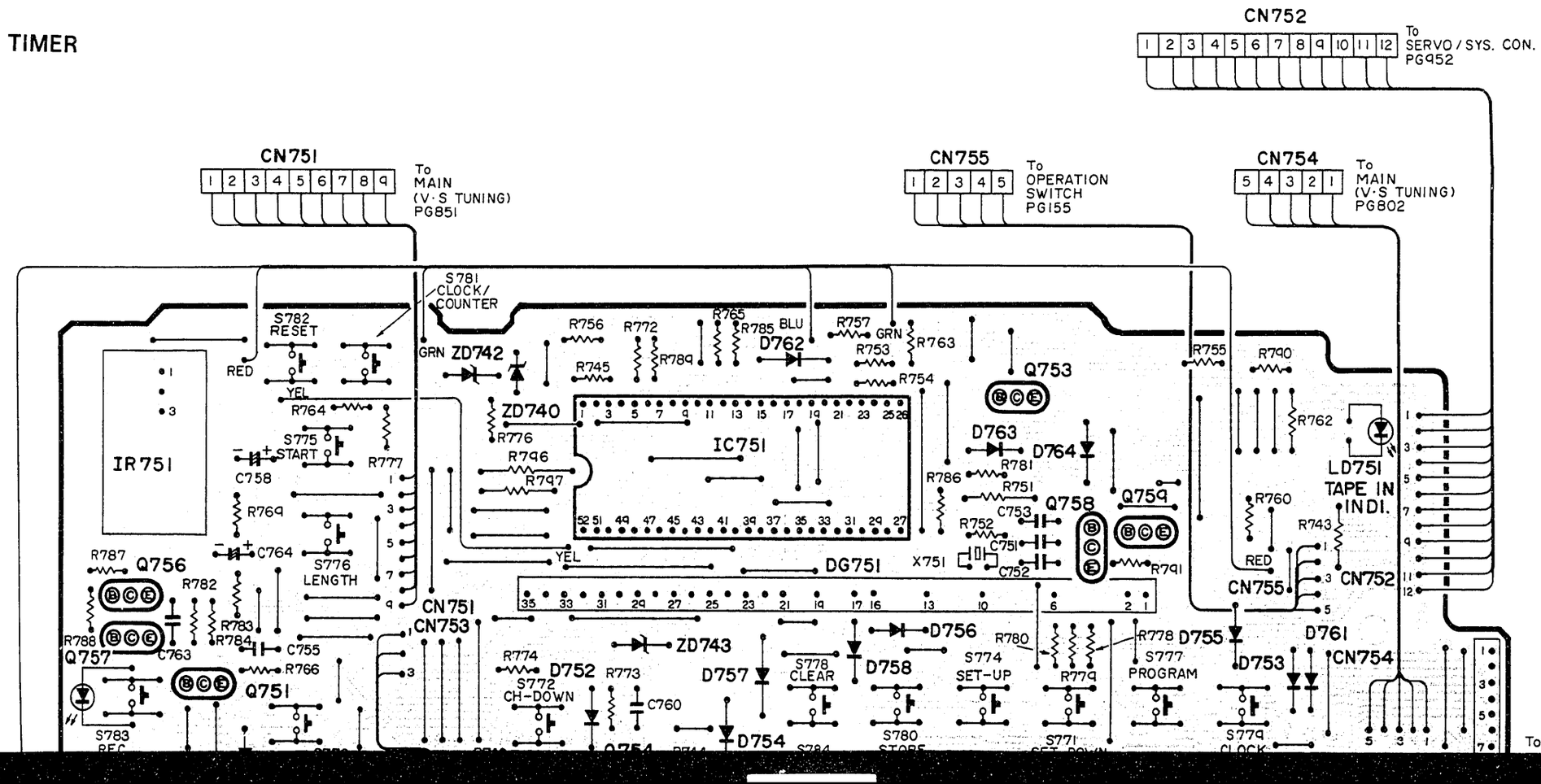
MAIN 5-19 5-20 MAIN

OPERATION SWITCH

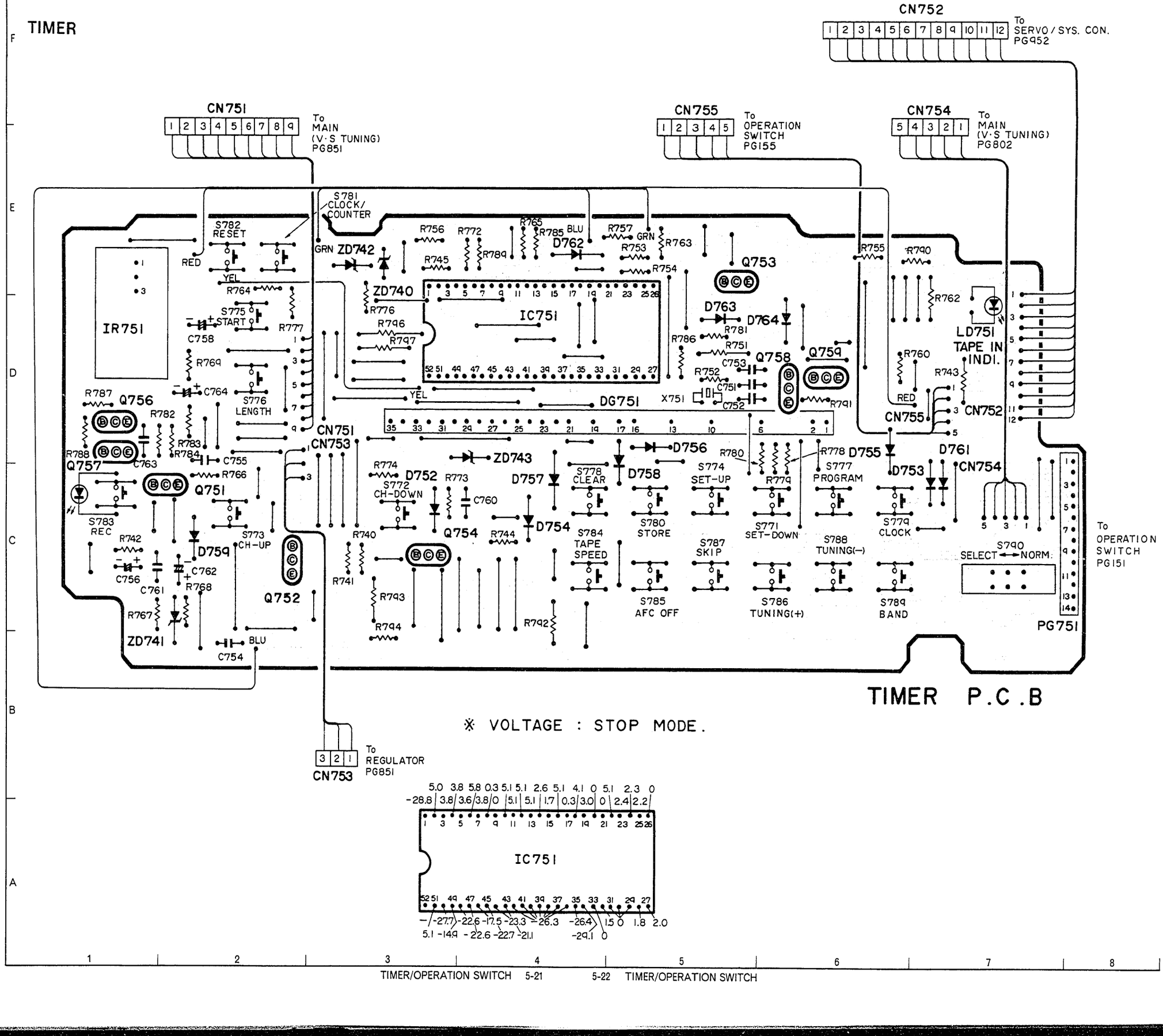


OPERATION SWITCH P.C.B

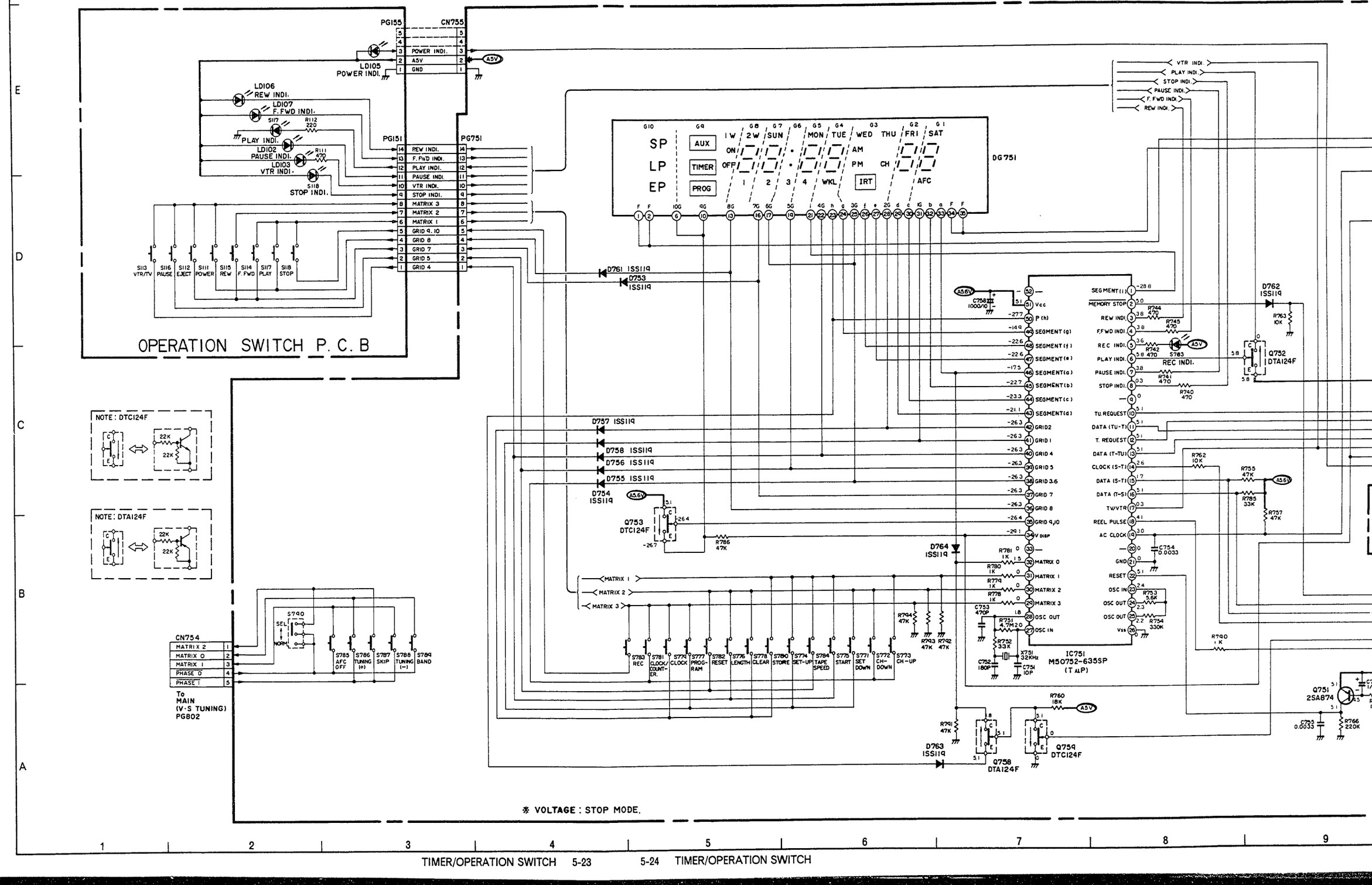
TIMER



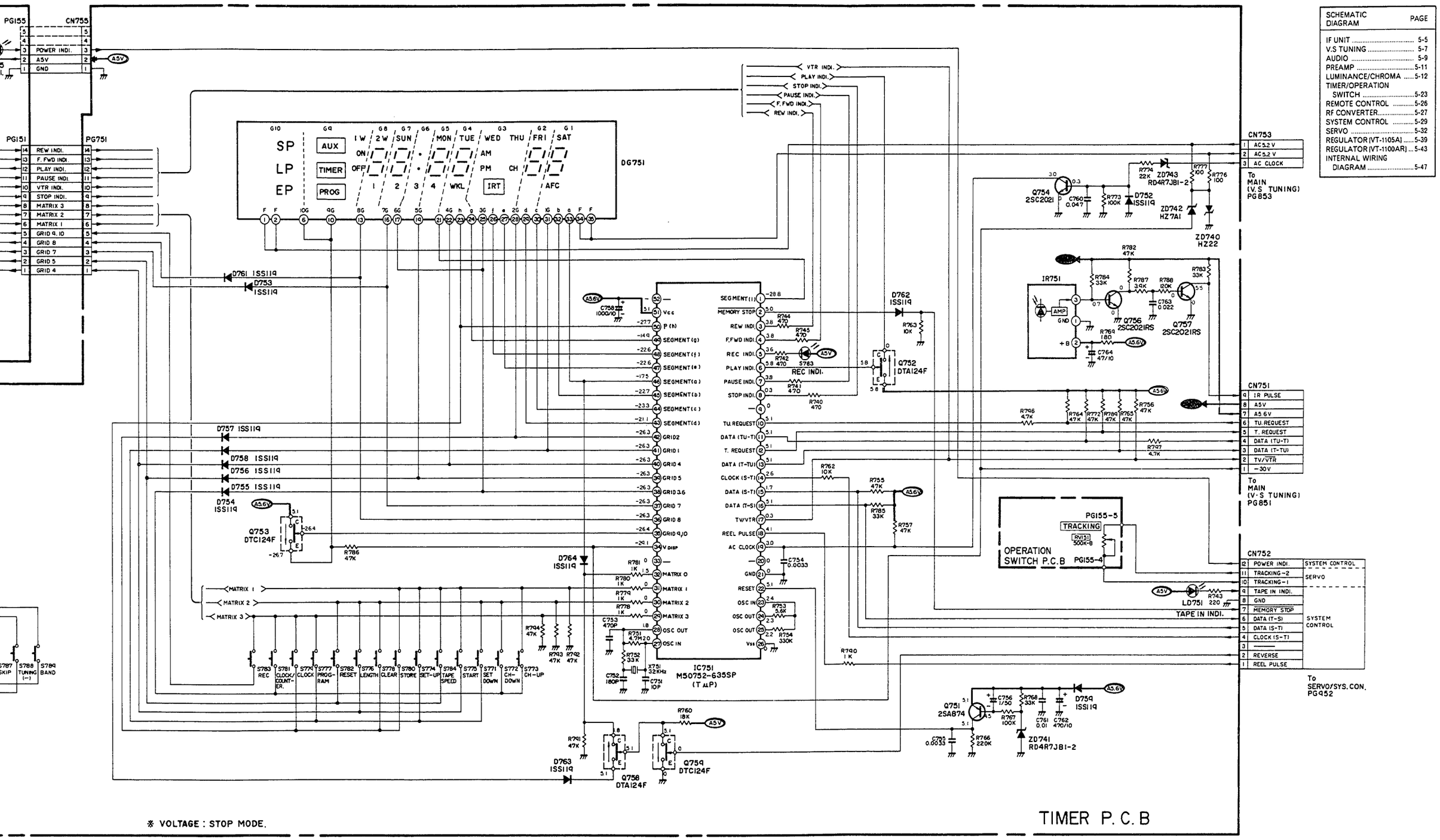
TIMER


CN752
1 2 3 4 5 6 7 8 9 10 11 12
To SERVO / SYS. CON. PG952
CN751
1 2 3 4 5 6 7 8 9
To MAIN (V·S TUNING) PG851
CN755
1 2 3 4 5
To OPERATION SWITCH PG155
CN754
5 4 3 2 1
To MAIN (V·S TUNING) PG802
S781 CLOCK/ COUNTER
S782 RESET
S775 START
S776 LENGTH
S783 REC
S772 CH-DOWN
S773 CH-UP
S774 SET-UP
S777 PROGRAM
S778 CLEAR
S779 CLOCK
S780 STORE
S771 SET-DOWN
S784 TAPE SPEED
S785 AFC OFF
S786 TUNING(+)
S787 SKIP
S788 TUNING(−)
S789 BAND
S790 SELECT ↔ NORM.
IR751
IC751
LD751 TAPE IN INDI.
X751
DG751
ZD740
ZD741
ZD742
ZD743
Q751
Q752
Q753
Q754
Q756
Q757
Q758
Q759
D752
D753
D754
D755
D756
D757
D758
D759
D761
D762
D763
D764
CN751
CN752
CN753
CN754
CN755
To OPERATION SWITCH PG151
PG751
TIMER P.C.B
※ VOLTAGE : STOP MODE.
3 2 1
To REGULATOR PG851
CN753
5.0 3.8 5.8 0.3 5.1 5.1 2.6 5.1 4.1 0 5.1 2.3 0
-28.8 3.8 3.6 3.8 0 5.1 5.1 1.7 0.3 3.0 0 2.4 2.2
1 3 5 7 9 11 13 15 17 19 21 23 25 26
IC751
52 51 49 47 45 43 41 39 37 35 33 31 29 27
— -27.7 -22.6 -17.5 -23.3 26.3 -26.4 1.5 0 1.8 2.0
5.1 -14.9 -22.6 -22.7 -21.1 -29.1 0
1 2 3 4 5 6 7 8
TIMER/OPERATION SWITCH 5-21
5-22 TIMER/OPERATION SWITCH

TIMER/OPERATION SWITCH



* VOLTAGE : STOP MODE.



SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
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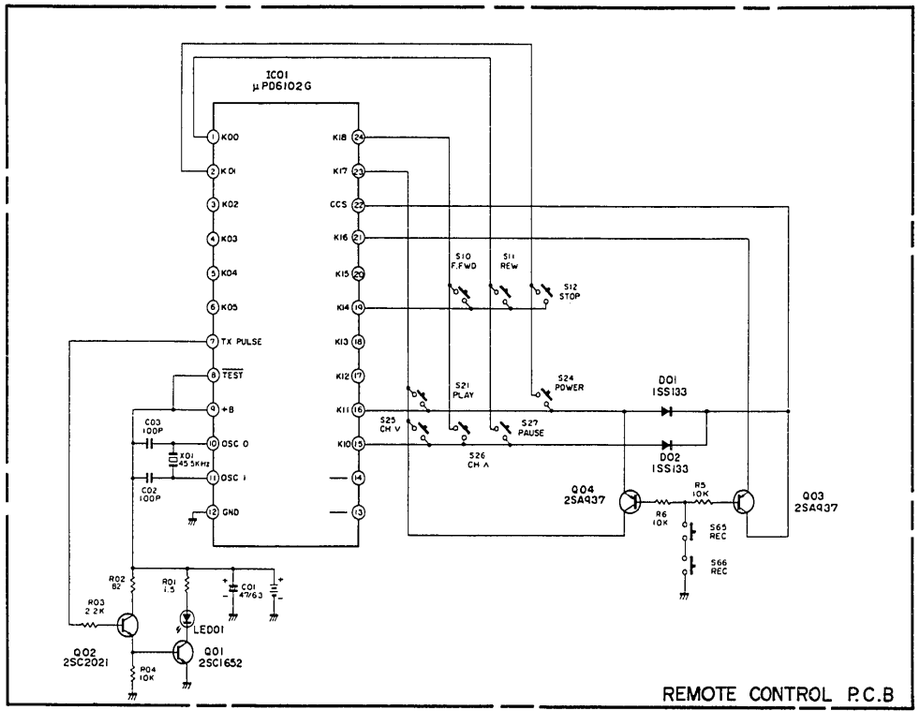
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

REMOTE CONTROL



SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
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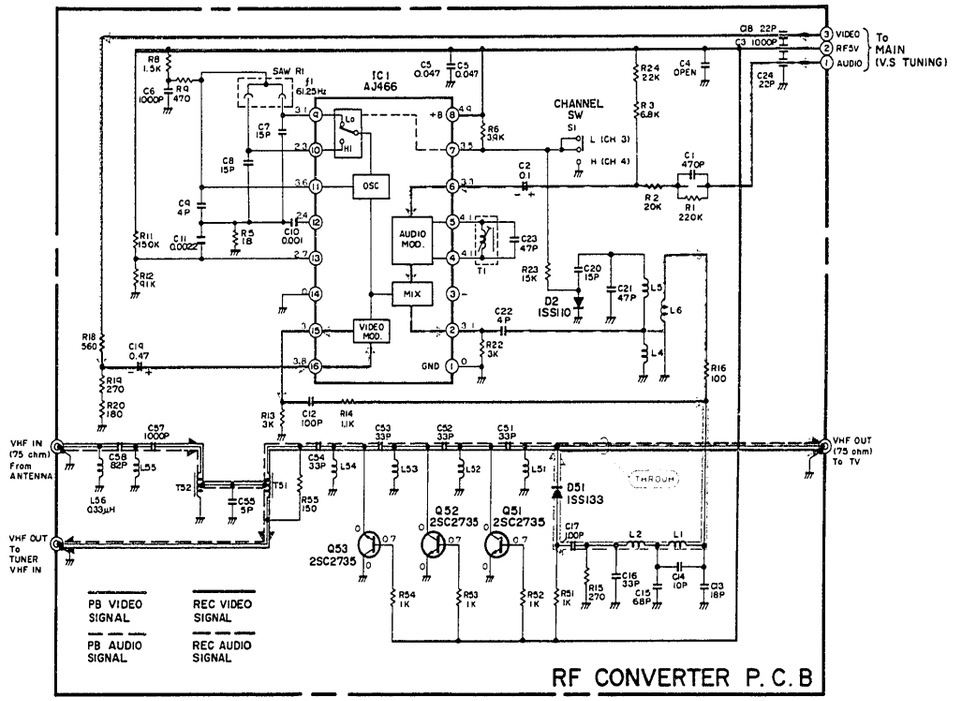
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

RF CONVERTER



※ VOLTAGE : PB OR REC MODE.

SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
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PREAMP	5-11
LUMINANCE/CHROMA	5-12
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REMOTE CONTROL	5-26
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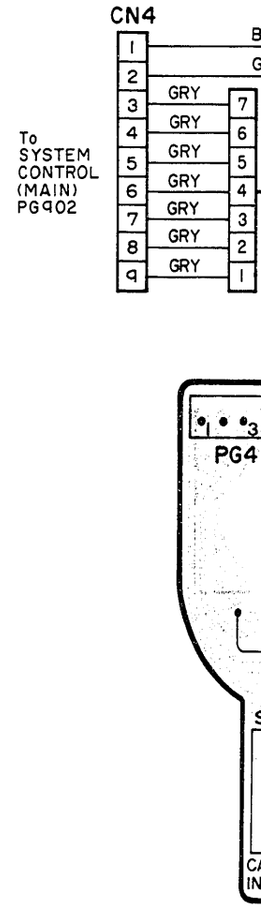
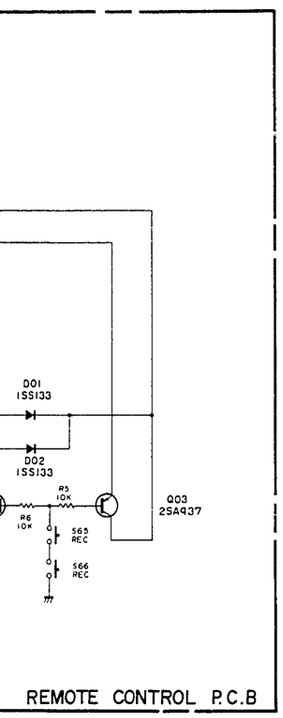
SERVO	5-32
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

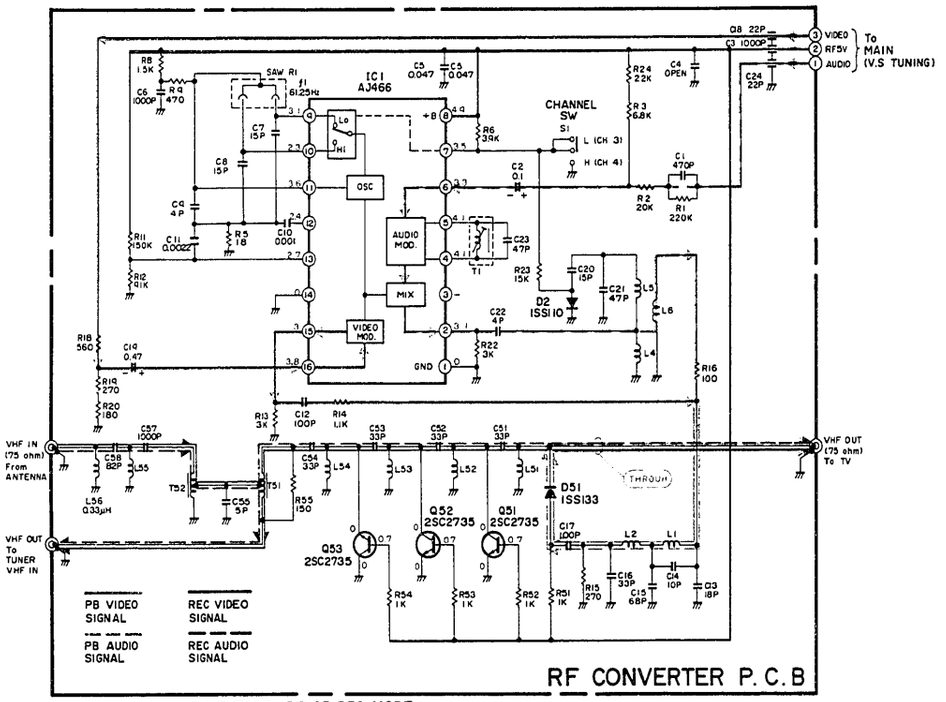
PERIPHERAL BOAR





REMOTE CONTROL P.C.B

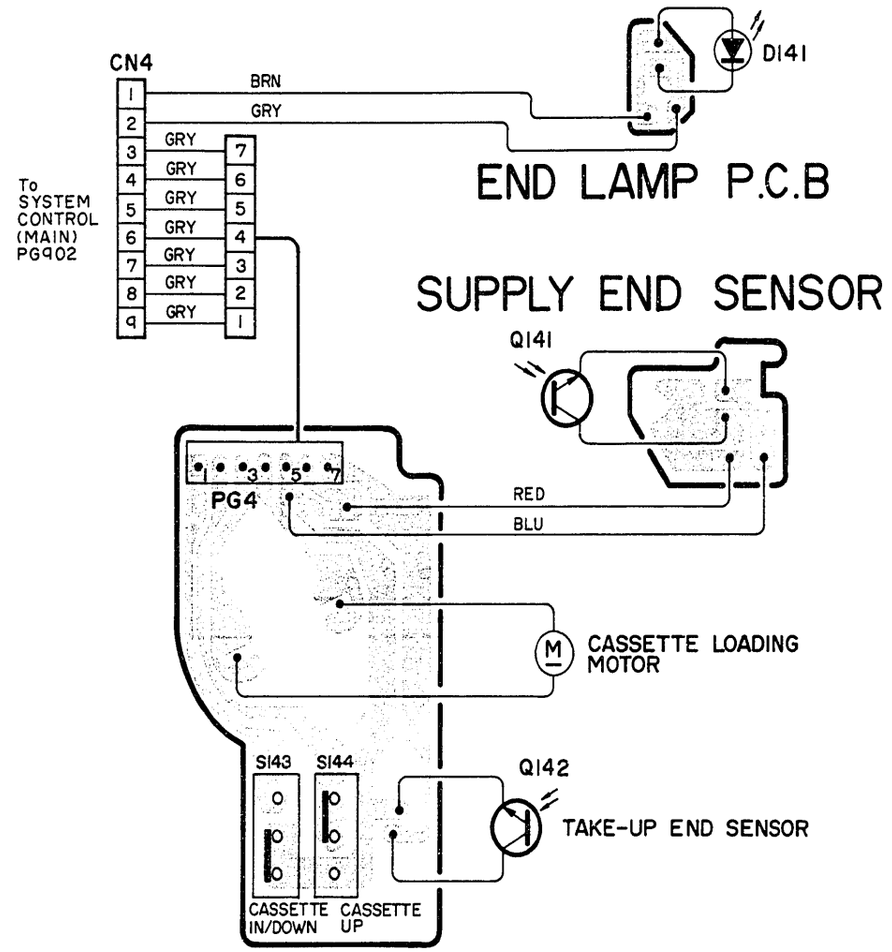
RF CONVERTER



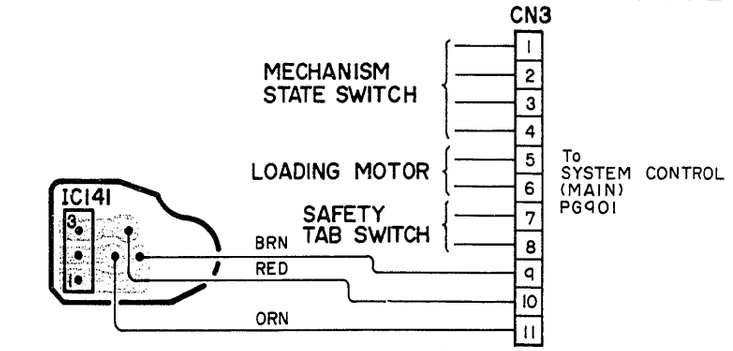
RF CONVERTER P.C.B

※ VOLTAGE : PB OR REC MODE.

PERIPHERAL BOARD



CASSETTE LOADING MOTOR P.C.B



TAKE-UP REEL SENSOR P.C.B

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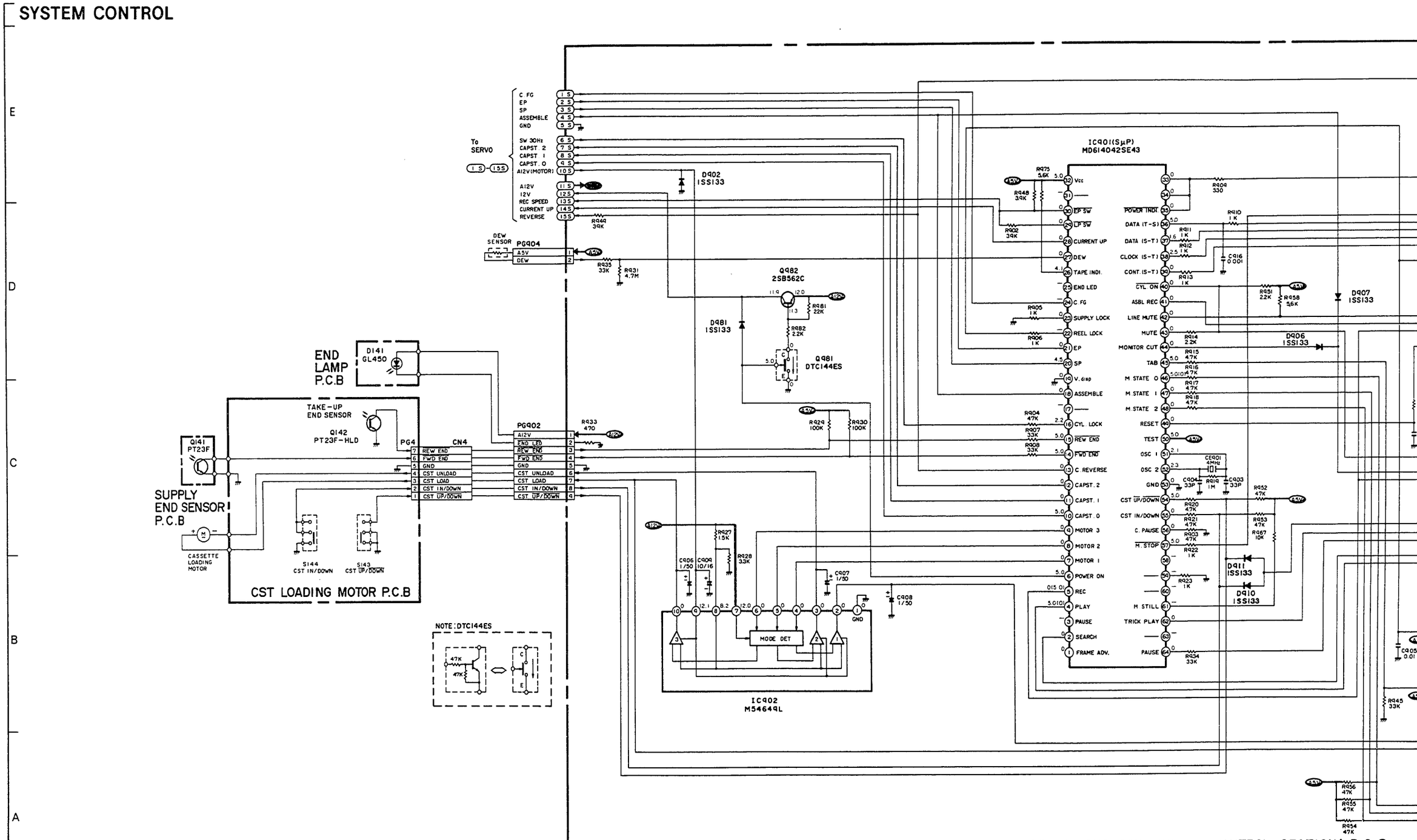
REGULATOR [VT-1105A]	5-39
REGULATOR [VT-1100AR]	5-43
INTERNAL WIRING DIAGRAM	5-47

SYSTEM CONTROL



※ ONE VOLTAGE : PB OR REC MODE, TWO VOLTAGES : PB AND (REC) MODE.

SCHEMATIC DIAGRAM	PAGE
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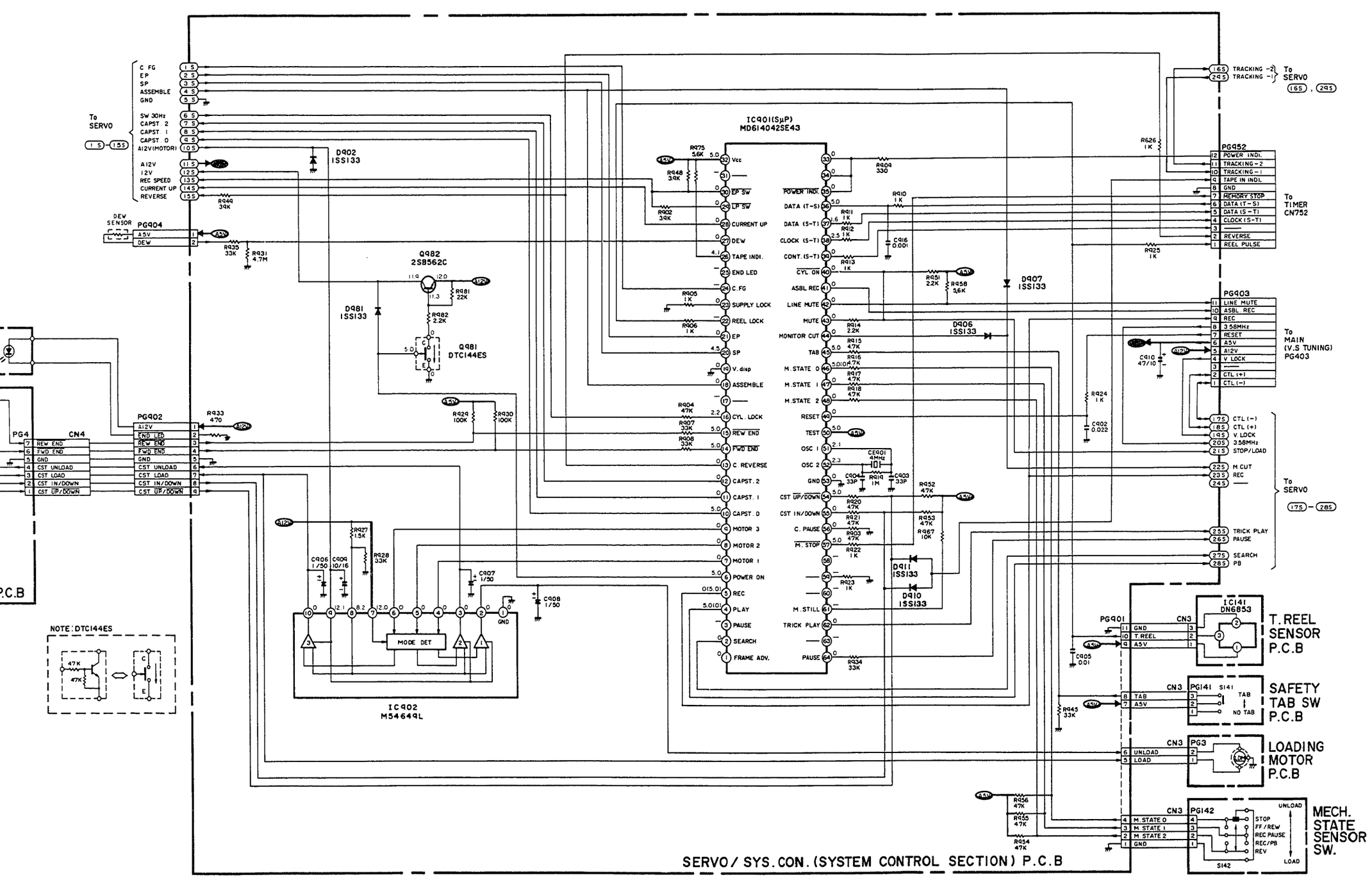
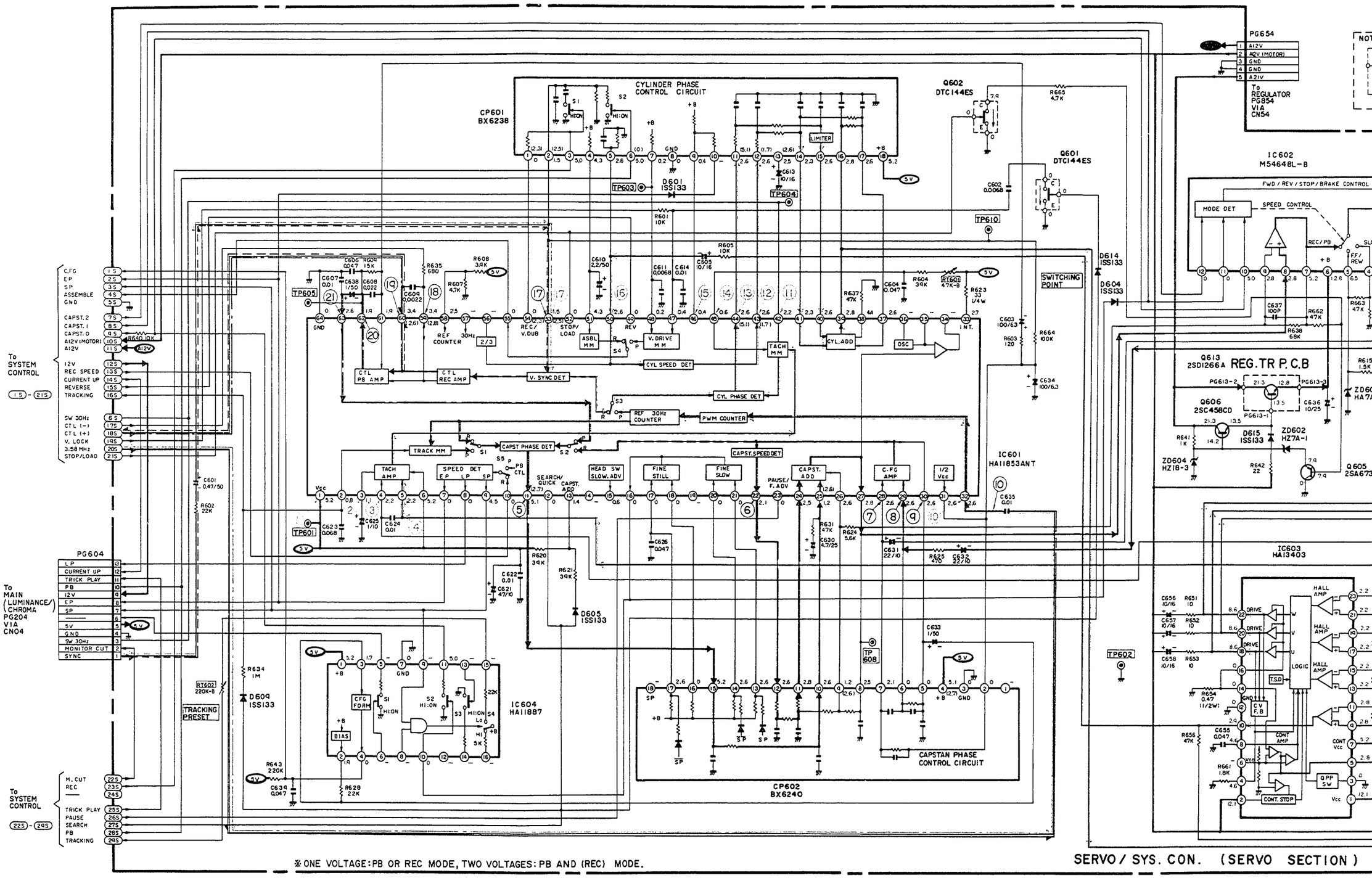
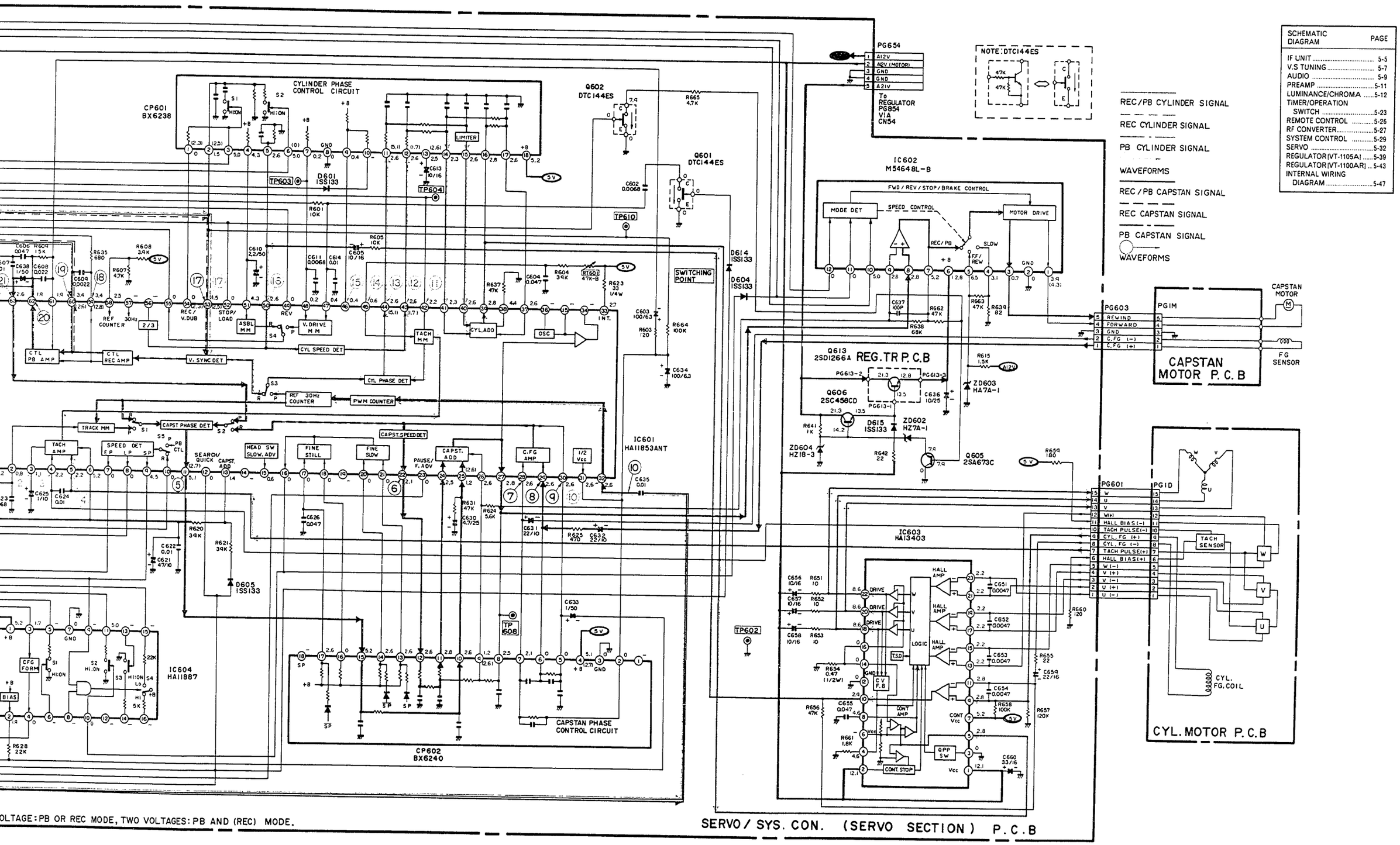
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47



※ ONE VOLTAGE : PB OR REC MODE, TWO VOLTAGES : PB AND (REC) MODE.



SERVO / SYS. CON. (SERVO SECTION)



SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
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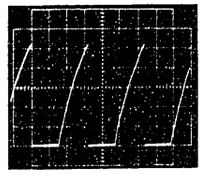
VOLTAGE: PB OR REC MODE, TWO VOLTAGES: PB AND (REC) MODE.

SERVO CIRCUIT WAVEFORMS

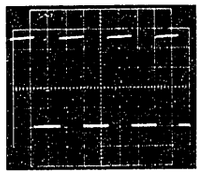
[IC601]

(REC: Color bar 1Vp-p Video IN/PB: NTSC Alignment tape)

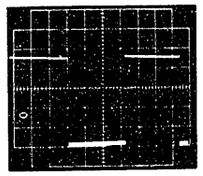
① PIN 2 REC/PB
0.5V/10ms. div.



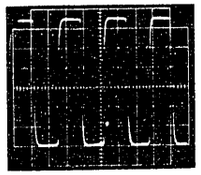
⑥ PIN 22 REC/PB
1V/0.1ms. div.



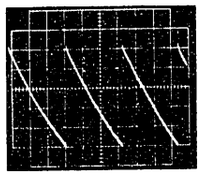
⑪ PIN 42 REC/PB
1V/5ms. div.



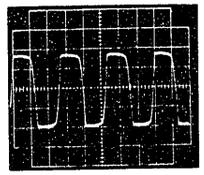
⑯ PIN 50 REC/PB
0.2V/1ms. div.



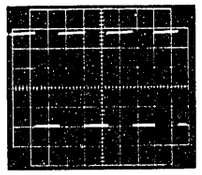
② PIN 3 REC/PB
0.1V/10ms. div.



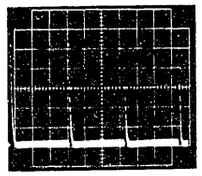
⑦ PIN 28 REC/PB
0.2V/0.5ms. div.



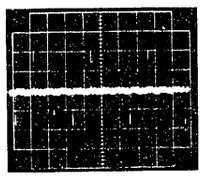
⑫ PIN 43 REC/PB
1V/0.2ms. div.



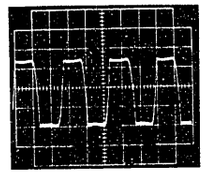
⑰ PIN 53 REC/PB
0.2V/5ms. div.



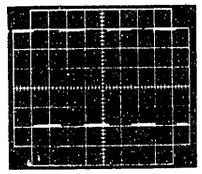
③ PIN 4 REC/PB
50mV/10ms. div.



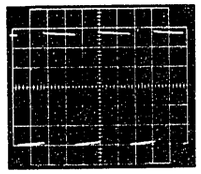
⑧ PIN 29 REC/PB
0.2V/0.5ms. div.



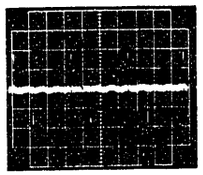
⑬ PIN 44 REC/PB
1V/0.2ms. div.



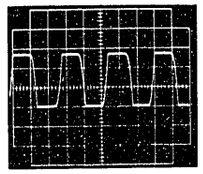
⑱ PIN 59 REC
0.5V/10ms. div.



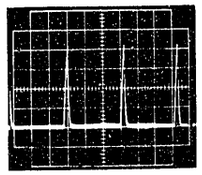
④ PIN 5 REC/PB
50mV/10ms. div.



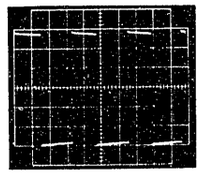
⑨ PIN 30 REC/PB
0.5V/0.5ms. div.



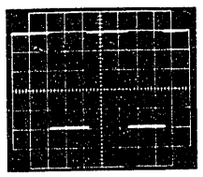
⑭ PIN 45 REC/PB
0.5V/5ms. div.



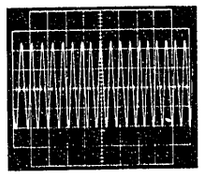
⑲ PIN 60 REC
0.5V/10ms. div.



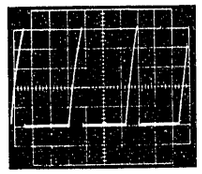
⑤ PIN 11 REC/PB
1V/0.5ms. div.



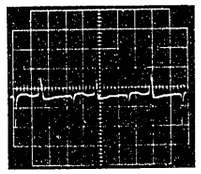
⑩ PIN 32 REC/PB
0.1V/0.5μs. div.



⑮ PIN 46 REC/PB
0.5V/5ms. div.



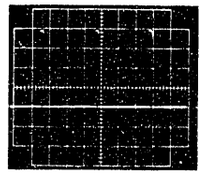
⑳ PIN62 (TP605) PB
1V/10ms. div.



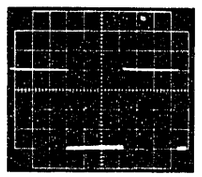
[IC601]

[TEST POINT]

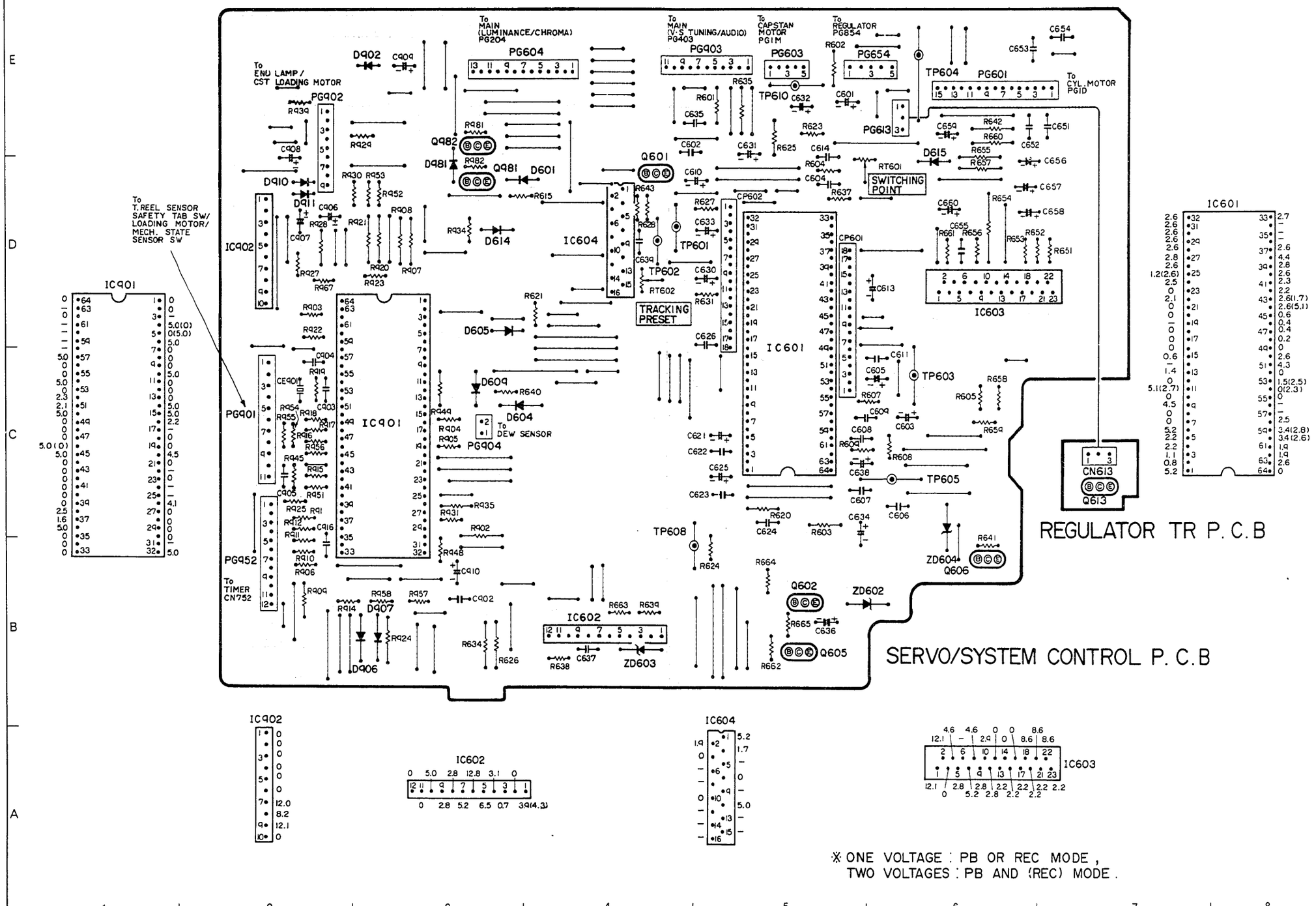
㉑ PIN 63 PB
1V/10ms. div.



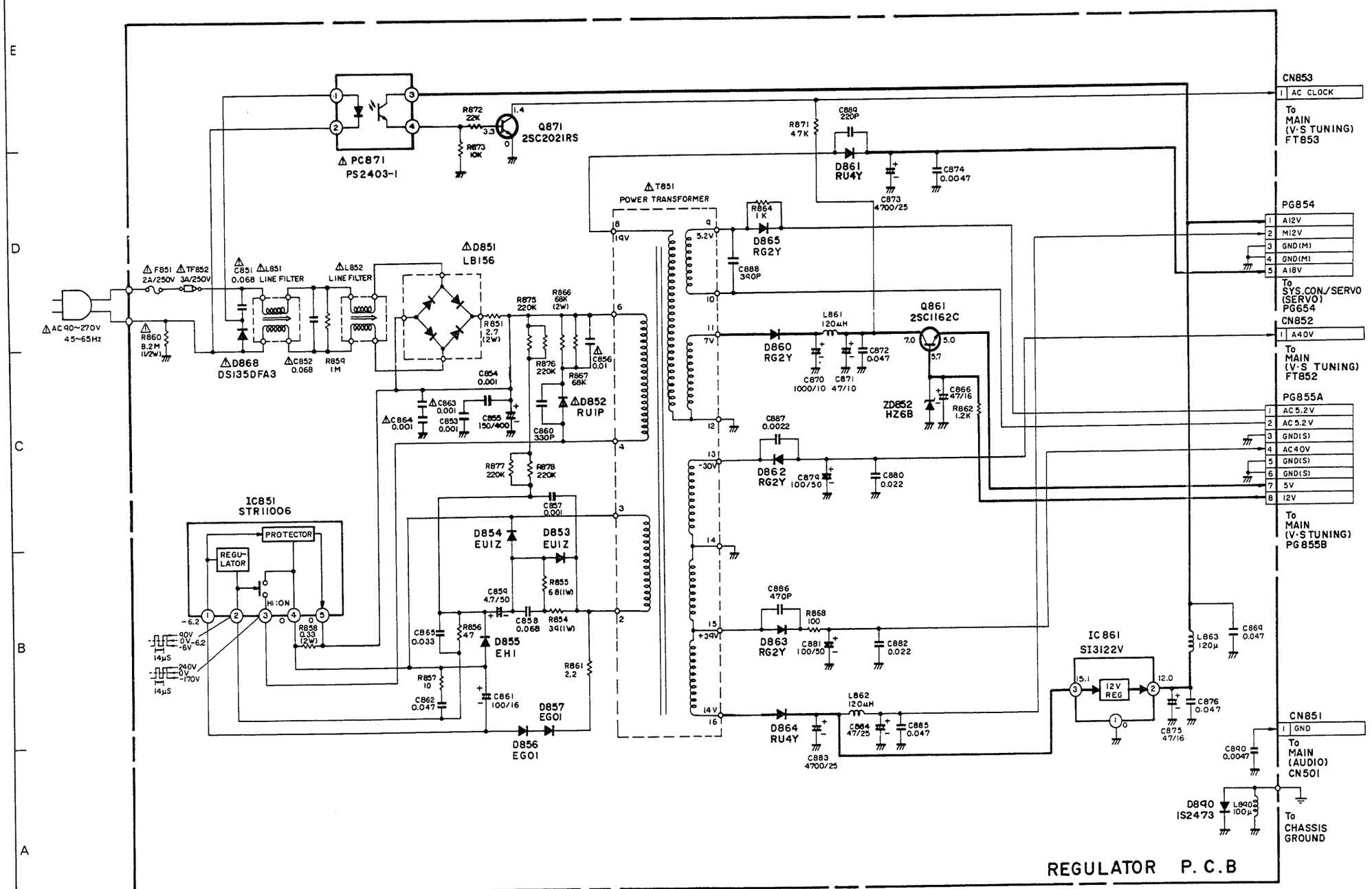
㉒ TP604 REC/PB
1V/5ms. div.



SERVO/SYSTEM CONTROL

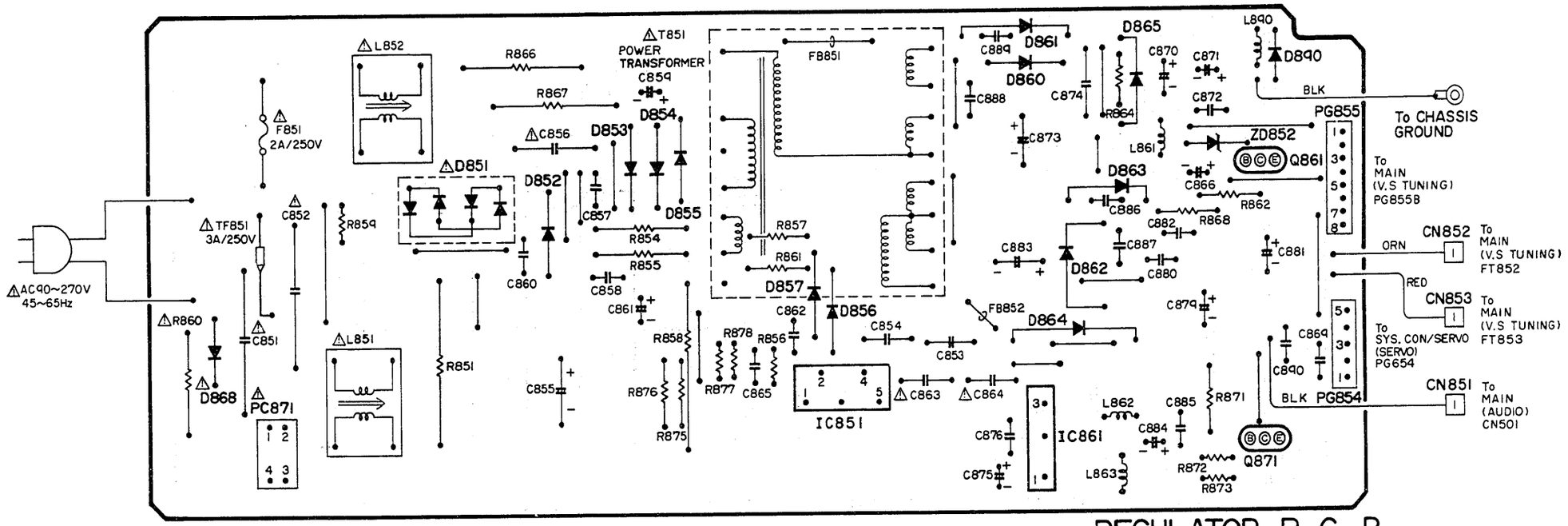


REGULATOR (VT-1105A)

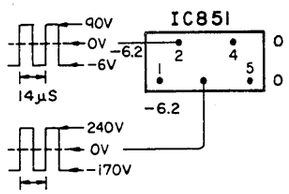


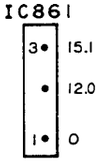
REGULATOR P. C. B

※ ONE VOLTAGE : PB OR REC MODE.



※ONE VOLTAGE : PB OR REC MODE.

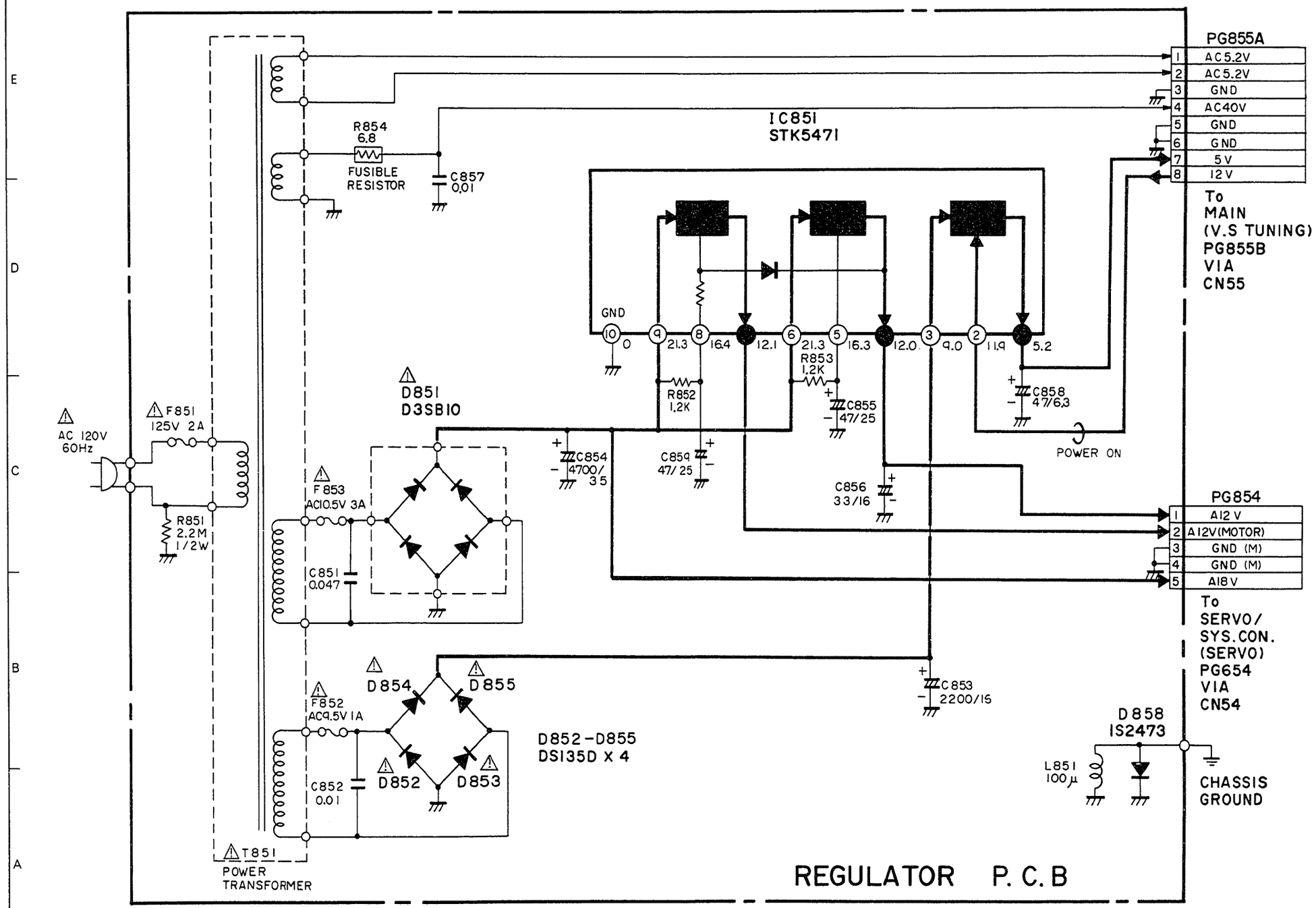


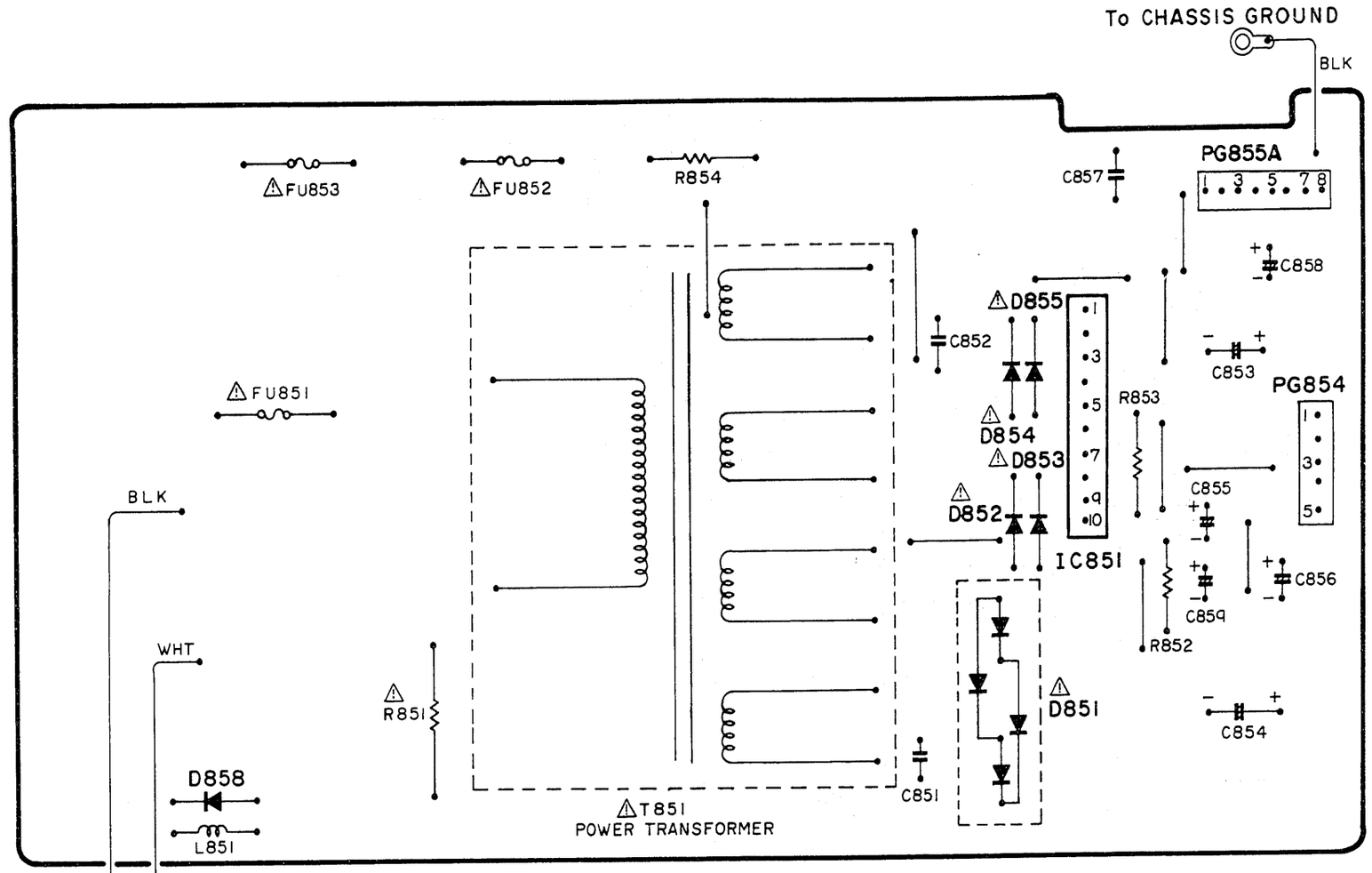


REGULATOR P. C. B

SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

REGULATOR (VT-1100AR)





REGULATOR P.C.B

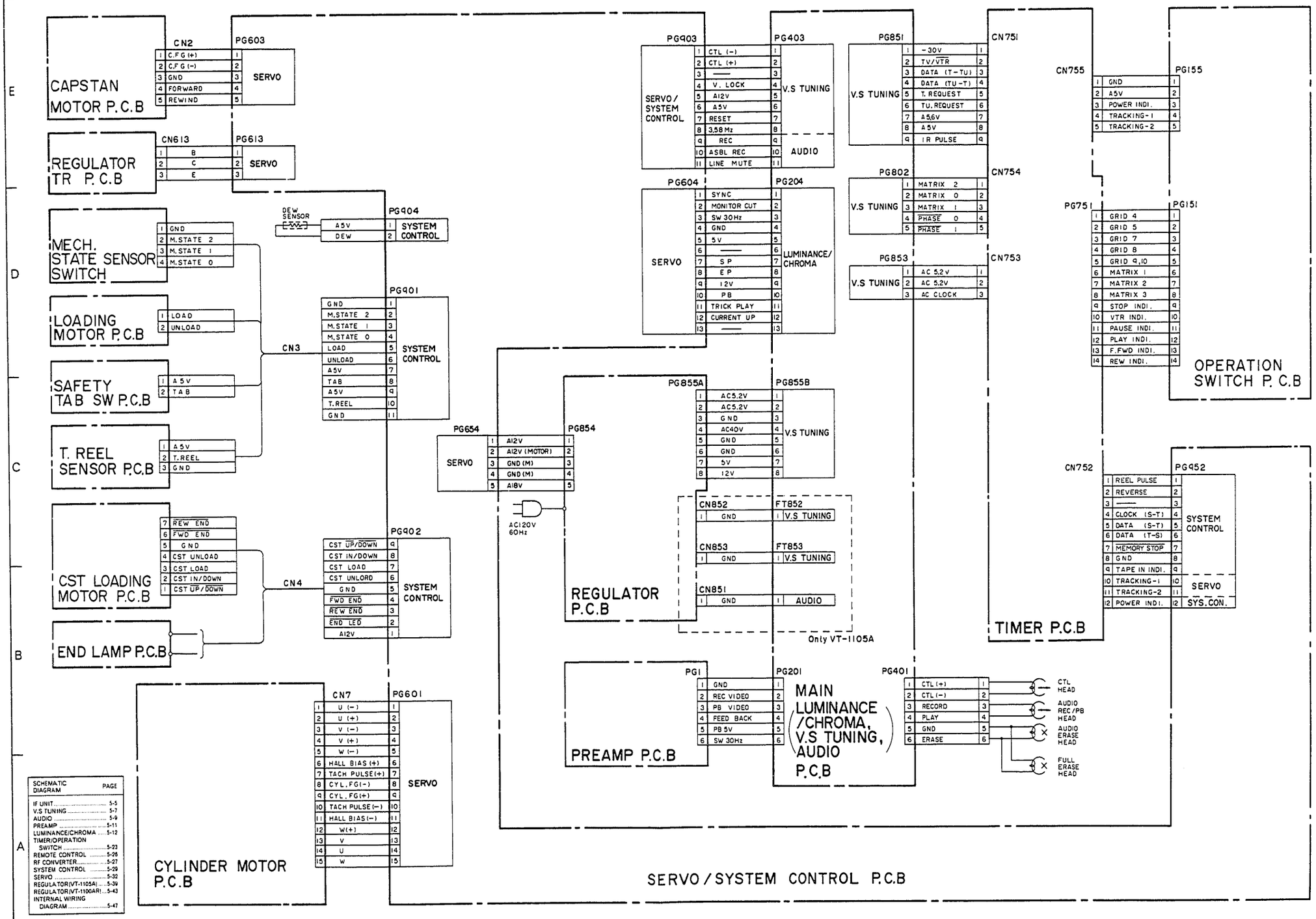
※ ONE VOLTAGE: PB OR REC MODE.

IC851

1	5.2
	11.9
3	9.0
	12.0
5	16.3
	21.3
7	12.1
	16.4
9	21.3
10	0

SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-26
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
SERVO	5-32
REGULATOR (VT-1105A)	5-39
REGULATOR (VT-1100AR)	5-45
INTERNAL WIRING DIAGRAM	5-47

INTERNAL WIRING DIAGRAM



SCHEMATIC DIAGRAM	PAGE
IF UNIT	5-5
V.S TUNING	5-7
AUDIO	5-9
PREAMP	5-11
LUMINANCE/CHROMA	5-12
TIMER/OPERATION SWITCH	5-23
REMOTE CONTROL	5-25
RF CONVERTER	5-27
SYSTEM CONTROL	5-29
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REGULATOR(VT-1105A)	5-39
REGULATOR(VT-1100AR)	5-43
INTERNAL WIRING DIAGRAM	5-47

REPLACEMENT PARTS LIST

ELECTRICAL PARTS LIST

SYMBOL-NO	P-NO	DESCRIPTION
		CAPACITORS
C 207	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 208	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 209	0208363	CERAMIC DISC 330PF+-10% 50V
C 213	0208360	CERAMIC DISC 100PF+-5% 50V
C 216	0208360	CERAMIC DISC 100PF+-5% 50V
C 228	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 232	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 234	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 235	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 237	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 239	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 241	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 242	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 247	0256194	ELECTROLYTIC 470MF,10V
C 248	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 249	0208348	CERAMIC DISC 10PF+-5% 50V
C 253	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 258	0208355	CERAMIC DISC 39PF+-5% 50V
C 259	0208358	CERAMIC DISC 68PF+-5% 50V
C 260	0208350	CERAMIC DISC 15PF+-5% 50V
C 261	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 262	0208375	CERAMIC DISC 0.022UF+-10% 50V
C 264	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 265	0208375	CERAMIC DISC 0.022UF+-10% 50V
C 266	0208375	CERAMIC DISC 0.022UF+-10% 50V
C 267	0208375	CERAMIC DISC 0.022μF+-10% 50V
C 409	0208369	CERAMIC DISC 220PF+-20% 50V
C 412	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 415	0208361	CERAMIC DISC 150PF+-10% 50V
C 417	0208371	CERAMIC DISC 4700PF+-20% 50V
C 422	0208376	CERAMIC DISC 2700PF+-20% 50V
C 429	0208374	CERAMIC DISC 0.01μF+-20% 50V
C 430	0208370	CERAMIC DISC 3300PF+-20% 50V
C 437	0208362	CERAMIC DISC 220PF+-10% 50V
C 513	0208363	CERAMIC DISC 330PF+-10% 50V
C 607	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 608	0208375	CERAMIC DISC 0.022UF+-10% 50V
C 609	0208369	CERAMIC DISC 2200PF+-20% 50V
C 622	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 624	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 635	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 637	0208360	CERAMIC DISC 100PF+-5% 50V
C 751	0208348	CERAMIC DISC 10PF+-5% 50V
C 753	0208364	CERAMIC DISC 470PF+-10% 50V
C 754	0208370	CERAMIC DISC 3300PF+-20% 50V
C 755	0208370	CERAMIC DISC 3300PF+-20% 50V
C 756	0256606	ELECTROLYTIC 1MF,50V
C 761	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 805	0209171	CERAMIC DISC 0.01μF+80-20% 50V
C 810	0208360	CERAMIC DISC 100PF+-5% 50V
C 811	0208354	CERAMIC DISC 33PF+-5% 50V
C 812	0208354	CERAMIC DISC 33PF+-5% 50V
C 814	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 817	0208375	CERAMIC DISC 0.022UF+-10% 50V
C 853	0256861	ELECTROLYTIC 2200μH 16V (VT-1100AR)
C 853	0256657	ELECTROLYTIC 4700μH 35V (VT-1100AR)
C 861	0256607	ELECTROLYTIC 47μH 25V (VT-1100AR)
C 861	0256783	ELECTROLYTIC 100MF,16V (VT-1105A)
C 863	0256622	ELECTROLYTIC 33MF 16V (VT-1100AR)
C 867	0256626	ELECTROLYTIC 47MF 6.3V (VT-1100AR)
C 870	0256858	ELECTROLYTIC 1000UF 10V (VT-1105A)
C 873	0256865	ELECTROLYTIC 3300UF 25V (VT-1105A)
C 875	0256627	ELECTROLYTIC 47MF,16V (VT-1105A)
C 887	0256860	ELECTROLYTIC 1000UF 25V (VT-1105A)
C 901	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 903	0208354	CERAMIC DISC 33PF+-5% 50V
C 904	0208354	CERAMIC DISC 33PF+-5% 50V
C 905	0208374	CERAMIC DISC 0.01UF+-20% 50V
C 906	0208374	ELECTROLYTIC 1MF, 50V
C 907	0208374	ELECTROLYTIC 1MF, 50V
C 908	0208374	ELECTROLYTIC 1MF, 50V
C 909	0208374	ELECTROLYTIC 10MF, 16V
		RESISTORS
R 654	0149705	RESISTOR METAL OXIDE 470 OHM
R 854	0170479	FOSE RESISTOR 6.80HM+-5% 1/4W (VT-1100AR)
R 854	0171028	OXIDE METAL FILM 390HM+-5% 1W (VT-1105A)
R 856	0171015	METAL FILM 47.HM+-5% 1W (VT-1105A)
RT 201	5007892	SEMI VARIABLE 220OHM
RT 202	5007897	SEMI VARIABLE 10KOHM
RT 401	5007898	SEMI VARIABLE 22KOHM
RT 402	5007902	SEMI VARIABLE 220KOHM
RT 501	5009143	VARIABLE 50KOHM
RT 601	5007899	SEMI VARIABLE 47KOHM
RV 151	5005901	RESISTOR VARIABLE
		SEMI-CONDUCTORS
D 203	5339021	DIODE 1SS133
D 204	5339021	DIODE 1SS133
D 206	5339021	DIODE 1SS133
D 210	5339021	DIODE 1SS133
D 402	5339131	DIODE 1SS254
D 501	5339021	DIODE 1SS133
D 502	5339021	DIODE 1SS133
D 601	5339021	DIODE 1SS133
D 604	5339021	DIODE 1SS133
D 605	5339021	DIODE 1SS133
D 609	5339021	DIODE 1SS133
D 615	5339021	DIODE 1SS133
D 752	5339071	DIODE 1SS119
D 753	5339071	DIODE 1SS119
D 754	5332681	DIODE 1SS119
D 755	5339071	DIODE 1SS119
D 756	5339071	DIODE 1SS119
D 757	5339071	DIODE 1SS119
D 758	5339071	DIODE 1SS119
D 759	5339071	DIODE 1SS119
D 760	5339071	DIODE 1SS119
D 761	5339071	DIODE 1SS119
D 762	5339071	DIODE 1SS119
D 763	5339071	DIODE 1SS119
D 764	5339071	DIODE 1SS119
D 801	5339171	DIODE 1SS130
D 802	5339171	DIODE 1SS130
D 803	5339131	DIODE 1SS254

SYMBOL-NO	P-NO	DESCRIPTION
		SEMI-CONDUCTORS
D 804	5339131	DIODE 1SS254
D 805	5339021	DIODE 1SS133
D 806	5339021	DIODE 1SS133
D 811	5339041	DIODE 1SS131
D 812	5339041	DIODE 1SS131
D 851	5332741	DIODE D3SB10 (VT-1100AR)
D 851	5333172	DIODE LB-156-B (VT-1105A)
D 852	5331671	DIODE DS135D (VT-1100AR)
D 853	5331671	DIODE DS135D (VT-1100AR)
D 853	5333161	DIODE EU1Z-G3 (VT-1105A)
D 854	5331671	DIODE DS135D (VT-1100AR)
D 854	5333161	DIODE EU1Z-G3 (VT-1105A)
D 855	5331671	DIODE DS135D (VT-1100AR)
D 855	5333211	DIODE EH1G3 (VT-1105A)
D 856	5333151	DIODE EG01-G3 (VT-1105A)
D 857	5333151	DIODE EG01-G3 (VT-1105A)
D 858	5330573	DIODE 1S2473 (VT-1100AR)
D 860	5333201	DIODE RG2Y-B3 (VT-1105A)
D 861	5333191	DIODE RU4Y-K1 (VT-1105A)
D 862	5333161	DIODE EU1Z-G3 (VT-1105A)
D 863	5333161	DIODE EU1Z-G3 (VT-1105A)
D 864	5333191	DIODE RU4Y-K1 (VT-1105A)
D 865	5333201	DIODE RG2Y-B3 (VT-1105A)
D 866	5333201	DIODE RG2Y-B3 (VT-1105A)
D 868	5331671	DIODE DS135D (VT-1105A)
D 902	5339021	DIODE 1SS133
D 906	5339021	DIODE 1SS133
D 907	5339021	DIODE 1SS133
D 981	5339021	DIODE 1SS133
IC 201	5373714	IC HT4765C
IC 202	5370972	IC HT4706A
IC 203	5367321	IC HA11888
IC 204	5362361	IC M5M6964
IC 205	5370961	IC HT4763
IC 206	5367311	IC M51485L
IC 401	5367581	IC M51654P
IC 501	5369431	IC LA7016
IC 601	5366082	IC HA11853NT
IC 602	5369913	IC M54648L-B
IC 603	5355584	IC HA13403
IC 604	5367481	IC HA11887
IC 751	5362909	IC M50752-635SP
IC 801	5362865	IC M50161-454SP
IC 802	5367341	IC LA7935
IC 803	5361071	IC M58657P
IC 851	5353651	IC STK5471 (VT-1100AR)
IC 851	5368421	IC STR11006 (VT-1105A)
IC 861	5366451	IC S1-3122V (VT-1105A)
IC 901	5361818	IC HD6140425E43
IC 902	5367111	IC M54649L
Q 201	5327063	TRANSISTOR 2SC1740S
Q 202	5327073	TRANSISTOR DTC144F
Q 203	5327031	TRANSISTOR 2SA673C
Q 204	5327073	TRANSISTOR DTC144F
Q 205	5327073	TRANSISTOR DTC144F
Q 207	5327063	TRANSISTOR 2SC1740S
Q 208	5327063	TRANSISTOR 2SC1740S

SYMBOL-NO	P-NO	DESCRIPTION
Q 401	5327101	TRANSISTER 2SC3553BC
Q 402	5327021	TRANSISTOR 2SA844CD
Q 403	5327111	TRANSISTER 2SC2784E
Q 404	5327111	TRANSISTER 2SC2784E
Q 405	5327073	TRANSISTOR DTC144F
Q 406	5327091	TRANSISTER 2SD1504E
Q 407	5321213	TRANSISTOR 2SD468C SILICON 190MHZ 0.9W
Q 408	5327073	TRANSISTOR DTC144F
Q 409	5327031	TRANSISTOR 2SA673C
Q 410	5721802	IC PROTECTER
Q 501	5327031	TRANSISTOR 2SA673C
Q 502	5327031	TRANSISTOR 2SA673C
Q 602	5327073	TRANSISTOR DTC144F
Q 605	5327031	TRANSISTOR 2SA673C
Q 606	5327001	TRANSISTOR 2SC458CD
Q 613	5323463	TRANSISTOR 2SD1266A
Q 751	5322883	TRANSISTOR 2SA874
Q 752	5323562	TRANSISTOR DTA124F
Q 753	5323561	TRANSISTOR DTC124F
Q 754	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W
Q 756	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W
Q 757	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W
Q 758	5323562	TRANSISTOR DTA124F
Q 759	5323561	TRANSISTOR DTC124F
Q 760	5323561	TRANSISTOR DTC124F
Q 801	5327001	TRANSISTOR 2SC458CD
Q 802	5327031	TRANSISTOR 2SA673C
Q 803	5327074	TRANSISTOR DTA144ES
Q 804	5327073	TRANSISTOR DTC144F
Q 861	5322733	TRANSISTOR 2SA952ML SILICON 160MHZ 0.6W (VT-1105A)
Q 862	5323561	TRANSISTOR DTC124F (VT-1105A)
Q 871	5321663	TRANSISTOR 2SC2021RS SILICON 180MHZ 0.3W (VT-1105A)
Q 902	5327073	TRANSISTOR DTC144F
Q 981	5327073	TRANSISTOR DTC144F
Q 982	5321203	TRANSISTOR 2SB562C
ZD 401	5339105	DIODE HZ7A1
ZD 602	5339105	DIODE HZ7A1
ZD 603	5339105	DIODE HZ7A1
ZD 604	5339107	DIODE HZ18-3
ZD 741	5332633	ZENNER DIODE RD4R7JSB1-2
ZD 742	5330322	DIODE HZ9B SI ZENER 1MHZ 0.4W
ZD 743	5332633	ZENNER DIODE RD4R7JSB1-2
ZD 801	5366151	IC UPC574J
ZD 802	5339108	DIODE HZ30
ZD 851	5330394	DIODE HZ6A2 SI ZENER 1MHZ 0.4W (VT-1105A)
		TRANSFORHERS
T 401	5262531	BIAS COIL
T 851	5272361	TRANSFORMER (VT-1105A)
T 851	5213733	TRANSFORMER (VT-1100AR)
		COILS
L 200	5159077	CHOKE COIL 100UH+-10%
L 201	5159089	CHOKE COIL 820UH+-10%
L 202	5159084	CHOKE COIL
L 203	5159077	CHOKE COIL 100UH+-10%
L 204	5159158	CHOKE COIL 220UH
L 205	5159143	CHOKE COIL 15UH

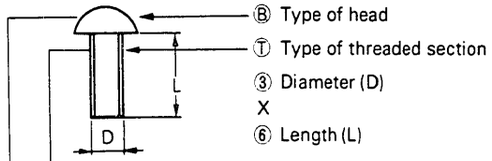
SYMBOL-NO	P-NO	DESCRIPTION
		COILS
L 206	5159145	CHOKE COIL 22UH
L 207	5159077	CHOKE COIL 100UH+-10%
L 210	5159084	CHOKE COIL
L 211	5159143	CHOKE COIL 15UH
L 212	5159077	CHOKE COIL 100UH+-10%
L 213	5159077	CHOKE COIL 100UH+-10%
L 214	5159143	CHOKE COIL 15UH
L 215	5159152	CHOKE COIL 68UH
L 216	5159158	CHOKE COIL 220UH
L 217	5159077	CHOKE COIL 100UH+-10%
L 401	5159089	CHOKE COIL 820UH+-10%
L 402	5159112	CHOKE COIL 2700UH
L 403	5159111	CHOKE COIL 5600UH
L 501	5159154	CHOKE COIL 100UH
L 851	5152472	CHOKE COIL 100UH (VT-1100AR)
L 851	5272291	LINE FILTER (VT-1105A)
L 861	5152751	CHOKE COIL 120UH+-10% (VT-1105A)
L 862	5152751	CHOKE COIL 120UH+-10% (VT-1105A)
		CRYSTALS
X 751	5780791	XTAL
X 801	5781571	CERAMIC OSC.
		MISCELLANEOUS
CE 901	5781571	CERAMIC OSC.
CP 202	5169011	BAND PASS FILTER
CP 203	5129002	TRAP COIL
CP 204	5169041	LOW PASS FILTER
CP 206	5169021	DELAY LINE
CP 601	5353871	BX6238
CP 602	5353891	BX6240
DG 751	5311833	DISPLAY
DL 201	5785823	DELAY LINE
F 851	5721406	FUSE (VT-1100AR)
F 851	5721476	FUSE (VT-1105A)
F 852	5721404	FUSE (VT-1100AR)

SYMBOL-NO	P-NO	DESCRIPTION
F 852	5721261	FUSE (VT-1105A)
F 852	5721408	FUSE (VT-1100AR)
IR 751	5490295	IR MODULE
LD 102	5380691	LED SLR34UR
LD 103	5380691	LED SLR34UR
LD 105	5380691	LED SLR34UR
LD 106	5380691	LED SLR34UR
LD 107	5380691	LED SLR34UR
LD 751	5380711	LED TLG123A
S 111	5635061	SWITCH
S 112	5635061	SWITCH
S 113	5634581	SWITCH
S 114	5634581	SWITCH
S 115	5634581	SWITCH
S 116	5634581	SWITCH
S 117	5634585	SWITCH
S 118	5634584	SWITCH
S 143	5633362	PUSH SWITCH
S 144	5633362	PUSH SWITCH
S 771	5635061	SWITCH
S 772	5635061	SWITCH
S 773	5635061	SWITCH
S 774	5635061	SWITCH
S 775	5635061	SWITCH
S 776	5635061	SWITCH
S 777	5635061	SWITCH
S 778	5635061	SWITCH
S 779	5635061	SWITCH
S 780	5635061	SWITCH
S 781	5635061	SWITCH
S 782	5635061	SWITCH
S 783	5634582	SWITCH
S 784	5635061	SWITCH
S 785	5635061	SWITCH
S 786	5635061	SWITCH
S 787	5635061	SWITCH
S 788	5635061	SWITCH
S 789	5635061	SWITCH
S 790	5622601	SWITCH

EXPLODED VIEWS

SCREW CLASSIFICATION

Example. BT3 × 6



Abbre-viation	Name	Shape
No symbol	Brazier head	
P	Pan head	
B	Binding head	
O	Oval countersunk head	
F	Flat countersunk head	

Abbre-viation	Name	Shape
No symbol	Machine (clamps without tapping)	
t	Tapping (clamps with tapping) Type 1	
T	Tapping (clamps with tapping) Type 2	
f	Forming tight (for metal)	

Note: Since the forming tight screw tightens while self-tapping machine screws can be replaced by tapping screws.

Washers and Nuts

Abbre-viation	Name	Shape
W	Washer	
SW	Spring washer	
LW	Locking washer	
E	E-ring	
N	Nut	

Note: Internal dia is indicated for nuts and washers.

LUBRICATION

Lubrication points are shown in the exploded view diagrams by marks (Ⓢ , Ⓗ)

Lubricants shown in the diagram are as follows.

Ⓢ Sonic slider oil (≒ 1600)

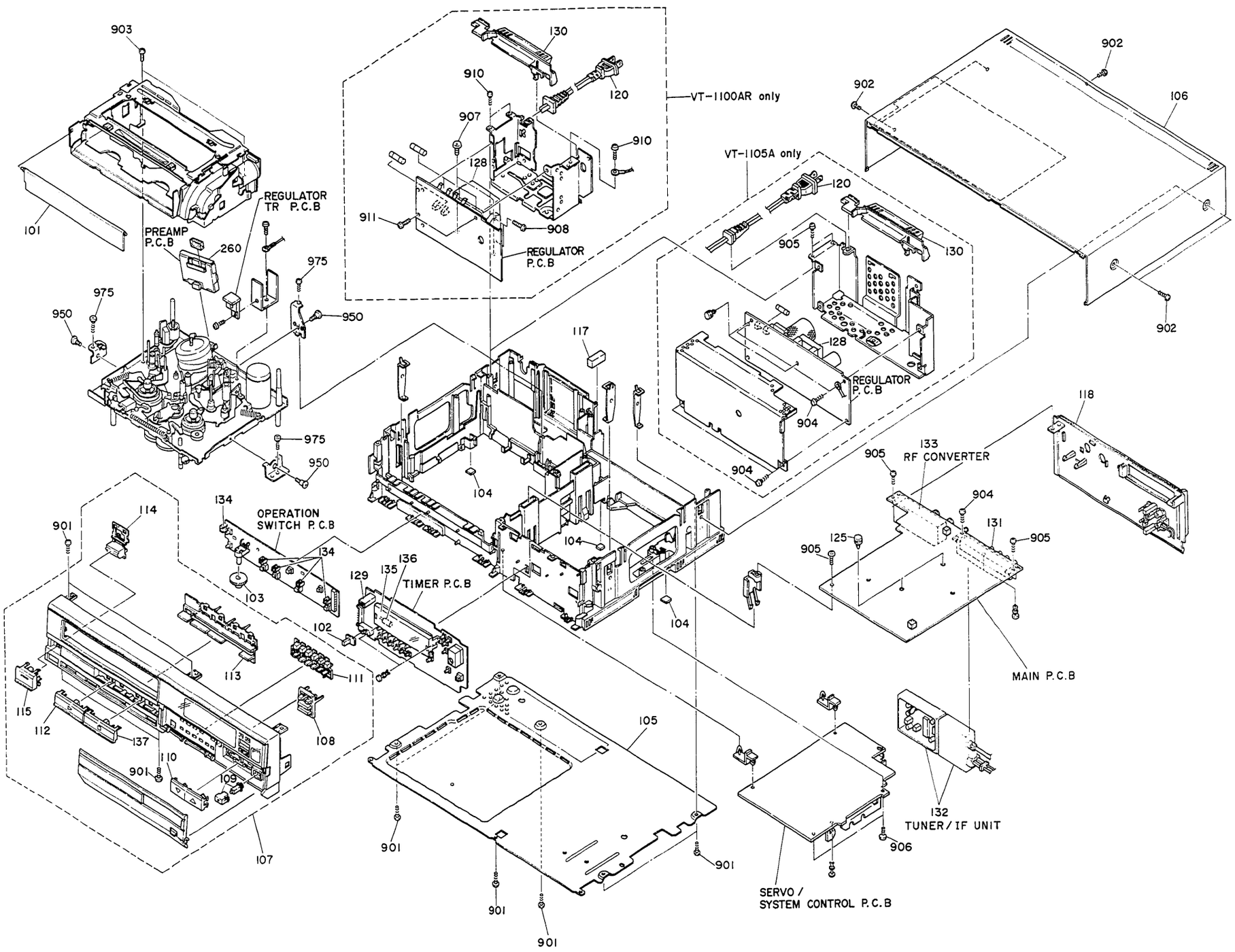
Ⓗ Hitazol (MO-138)

MECHANICAL PARTS LIST

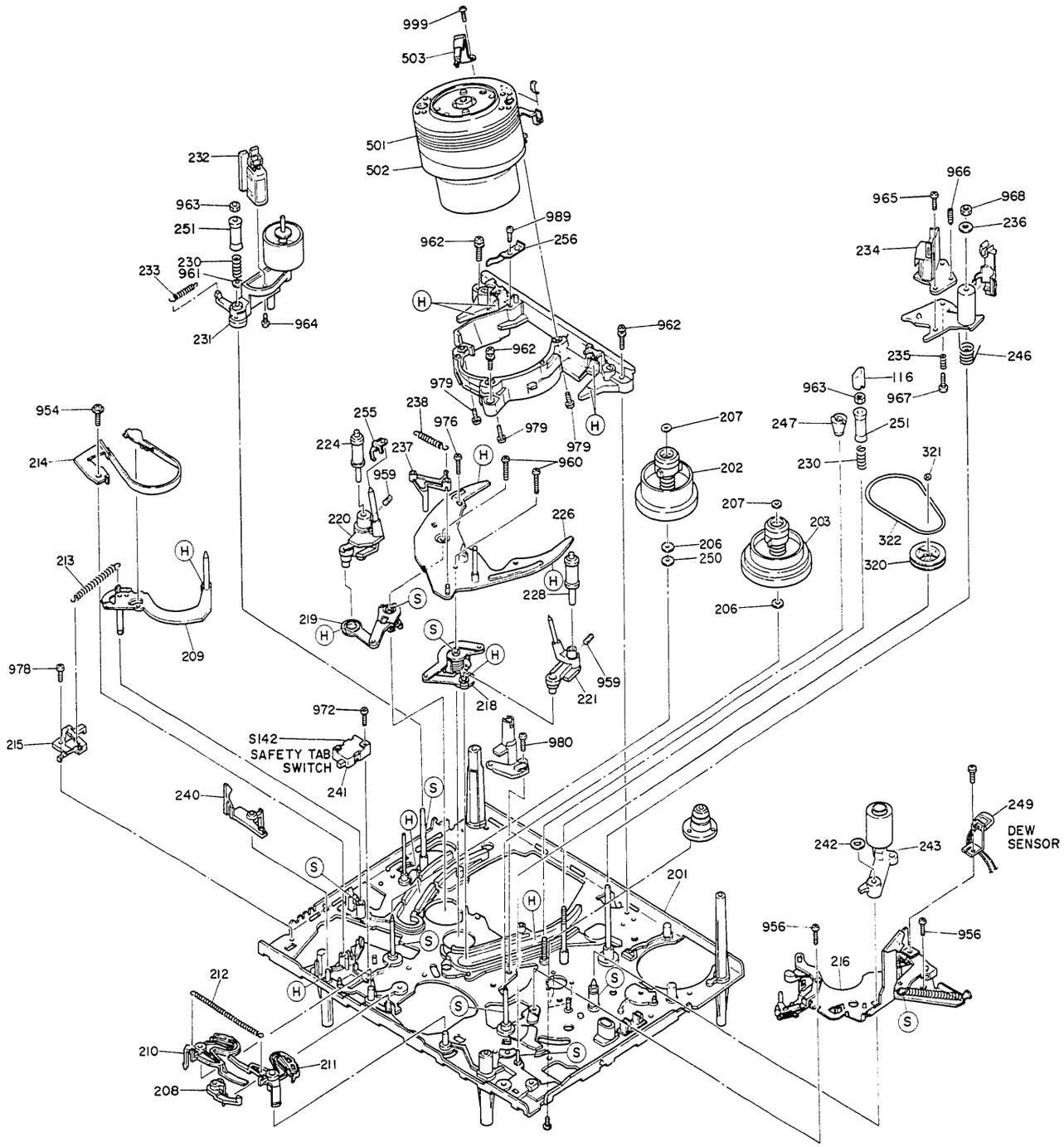
SYMBOL-NO	P-NO	DESCRIPTION
		FOR FINAL ASSEMBLY
101	6189382	CASSETTE DOOR
102	6084991	BUTTON-TRACKING
103	6077641	TRACKING KNOB (VT-1100AR)
103	6077643	TRACKING KNOB (VT-1105A)
104	7741444	FELT (LEG)
105	6000884	BOTTOM COVER
106	6001896	COVER (VT-1100AR)
106	6001862	COVER (VT-1105A)
107	6238326	FRONT PANEL (VT-1100AR)
107	6238327	FRONT PANEL (VT-1105A)
108	6083802	BUTTON
109	6085502	BUTTON-RECORD
110	6084151	BUTTON-CHANNEL
111	6084984	BUTTON
112	6085712	BUTTON-PLAY
113	6085962	BUTTON-FUNCTION (VT-1100AR)
113	6085963	BUTTON-FUNCTION (VT-1105A)
114	6084134	BUTTON-EJECT (VT-1100AR)
114	6084133	BUTTON-EJECT (VT-1105A)
115	6084091	BUTTON-POWER
116	6864241	CAP
117	6592111	CAP
118	5687726	REAR TERMINAL
119	6894011	CBA PIECE
120	5746876	POWER CORD (VT-1100AR)
120	585061	POWER CORD (VT-1105A)
124	6893831	HINGE
125	6890501	STUB
128	5213733	TRANSFORMER (VT-1100AR)
128	5272361	TRANSFORMER (VT-1105A)
129	6892861	LED HOLDER
130	6892511	REAR PIECE
131	5672492	JACK PLATE
132	5586504	TUNER IF BLOCK
133	5587573	RF CONVERTOR
134	6875561	HOLDER
135	6886062	DISPLAY HOLDER
136	6869311	COVER
137	6085052	BUTTON
202	6415391	REEL TABLE-SUPPLY
203	6415412	REEL TABLE-TAKE UP
206	7787412	WASHER
207	7778859	POLYSLIDER WASHER
208	6865662	ARM-BRAKE
209	7386841	TENSION ARM
210	6865804	BRAKE L
211	6865812	BRAKE R
212	6302471	SPRING
213	6543864	SPRING
214	7376271	TENSION BAND
215	6879421	BT.SPRING HOLDER
216	7386882	ARM BRACKET
217	6886792	ARM
218	7376303	LOADING LINK (RIGHT) ASSEMBLY
219	7376313	LOADING LINK (LEFT) ASSEMBLY
220	6978301	GUIDE ROLLER BASE (I)
221	6974661	BASE
224	6869481	GUIDE ROLLER
226	7386892	GUIDE BASE HOLDER
228	6868061	GUIDE ROLLER ASSEMBLY (OUT)
230	6304903	SPRING
231	6879902	IMPEDANCE ARM ASSEMBLY
232	5446151	FULL ERASE HEAD
233	6302391	SPRING
234	5446091	AUDIO CONTROL HEAD
235	6304906	SPRING
236	7786245	WASHER
237	6878932	SUB BRAKE
238	6300084	SPRING
239	5578761	MOTOR-CAPSTAN
240	6865675	RECORDING PREVENTION ARM
241	5633971	SWITCH (S142)
242	7788143	POLYSLIDER WASHER
243	6975471	ARM
246	6547811	SPRING
247	6979042	SCREW
248	5625141	SWITCH
249	5372671	DEW SENSOR
250	6873291	COLLAR
251	4504401	TAPE GUIDE
255	6877521	COLLAR
256	6539101	SPRING
259	7786626	WASHER
260	5372131	PRE AMP PCB ASSEMBLY
301	6886824	CLUCH PLATE ASSEMBLY
302	6355561	BELT
303	7386971	SLIDER-BRAKE
304	6865733	MODE SLIDER
305	6547821	SPRING
306	6889552	GEAR
307	6865791	TENTION ARM
311	7386933	LOADING MOTOR
312	6356111	BELT
313	6356451	BELT
314	6979051	FLYWHEEL
315	7788142	POLYSLIDER WASHER (THRUST)
316	7788861	WASHER
317	6356101	BELT
318	6356081	BELT
319	7386833	PLATE
320	6869291	PULLEY
321	7778859	POLYSLIDER WASHER
322	6355561	BELT
401	7397054	FRONT LOADING MECHA ASSEMBLY
402	7386745	SIDE BRACKET (L) ASSEMBLY
403	7386701	BRACKET(R)
404	7386815	CASSETTE HOLDER
412	7394493	BRACKET-MOTOR
414	5946911	MOTOR CBA
417	6879104	LOADING GEAR ASSEMBLY (R)
423	6879093	LOADING GEAR ASSEMBLY (L)
424	7367361	PLATE
425	6887322	FRONT HOLDER
426	4500402	SHAFT
427	6879153	DOOR ARM
428	6301027	SPRING

SYMBOL-NO	P-NO	DESCRIPTION
		FOR FINAL ASSEMBLY
430	6879182	GUIDE PIECE
501	5459781	UPPER CYLINDER
502	5459791	LOWER CYLINDER
503	5792631	BRUSH
901	8699410	BT BIND HEAD SCREW 3MMD X 14MM BLACK
902	7784428	SCREW (M3)
903	8671406	SCREW
904	8691408	SCREW (VT-1100AR)
905	8699410	BT BIND HEAD SCREW 3MMD X 14MM BLACK
906	8699412	BIND TAPPING SCREW-3MMX12MM (BLACK)
907	8691608	SCREW (VT-1100AR)
908	8691414	SCREW (VT-1100AR)
910	8699410	SCREW (VT-1100AR)
911	8691408	SCREW (VT-1100AR)
950	7541395	SPECIAL SCREW
951	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
952	8741408	SCREW (B3X8)
954	7781133	BT SCREW 3MMD
955	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
956	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
958	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
959	7773083	SCREW
960	8741408	SCREW (B3X8)
961	8812114	WASHER - 3MMD SMALL
962	7784293	SCREW (3MM)
963	8821114	3D NUT
964	8741103	SCREW(2X3B)
965	7781872	SCREW-3MMDX8MM
966	7773086	SCREW
967	8741414	BINDING SCREW - 3MMD X 14MM
968	8821114	3D NUT
969	8741408	SCREW (B3X8)
970	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
971	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
972	8691312	BT BIND SCREW-2.6MMDX12MM
975	8699410	BT BIND HEAD SCREW 3MMD X 14MM BLACK
976	7782781	SCREW 3X8BT
977	8691408	BIND HEAD TAPPING SCREW 3MMD X 8MM
978	8741408	SCREW (B3X8)
979	7784292	SCREW (3MM)
980	8741406	BIND SCREW - 3MMD X 6MM
983	8741403	BIND SCREW-3MMDX3MM
985	8671406	SCREW
986	8678405	DT SCREW-3MMDX5MM (BLACK)
988	8691410	SCREW
989	8691105	SCREW
990	8741406	BIND SCREW - 3MMD X 6MM
991	8741406	BIND SCREW - 3MMD X 6MM
		FOR ACCESSARIES
803	5638733	REMOTE CONTROL UNIT
804	5893174	CONNECTOR
805	5687871	300-750HM VHF ANTENNA ADAPTER
806	5855271	CABLE

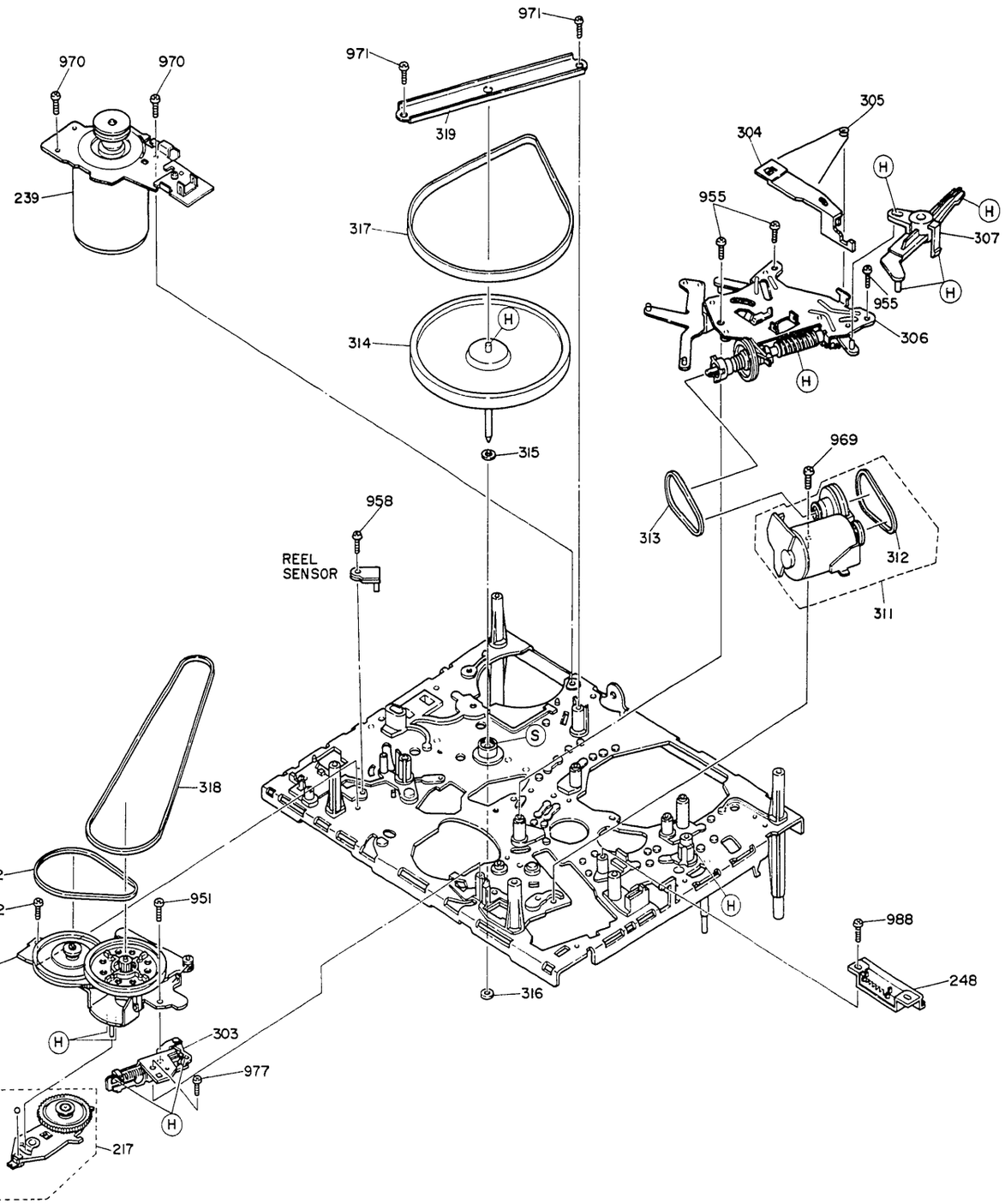
CABINET ASSEMBLY



CHASSIS ASSEMBLY (I)



CHASSIS ASSEMBLY (II)



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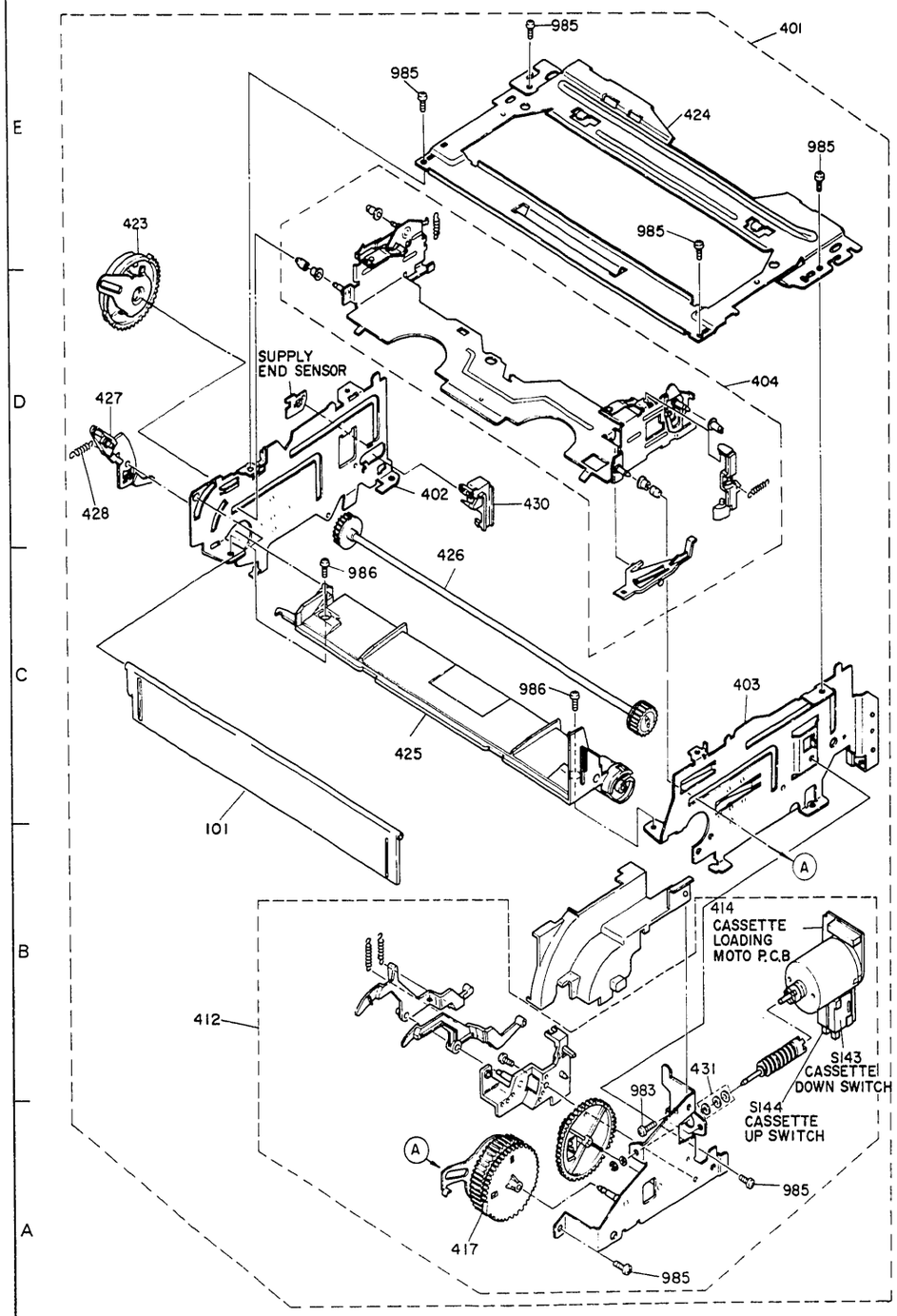
CASSETTE LOADING MECHANISM ASSEMBLY



CYLINDER MOTOR ASSEMBLY